

Compal Confidential

STORM2 M/B Schematic

LA-E292P

<https://vinafix.com>

Rev: 0.1_E

2016.05.03

| | | | | | |
|---|--|--------------------|--|--------------------------|-----------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | | Deciphered Date | | Title | |
| 2014/11/04 | | 2016/12/31 | | COVER PAGE | |
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| | | | | Document Number | 0.1 |
| | | | | Date | |
| | | | | Custom | LA-E292P |
| | | | | Custody | Tuesday, May 03, 2016 |
| | | | | Sheet | 1 of 75 |

STORM 2 Block-Diagram

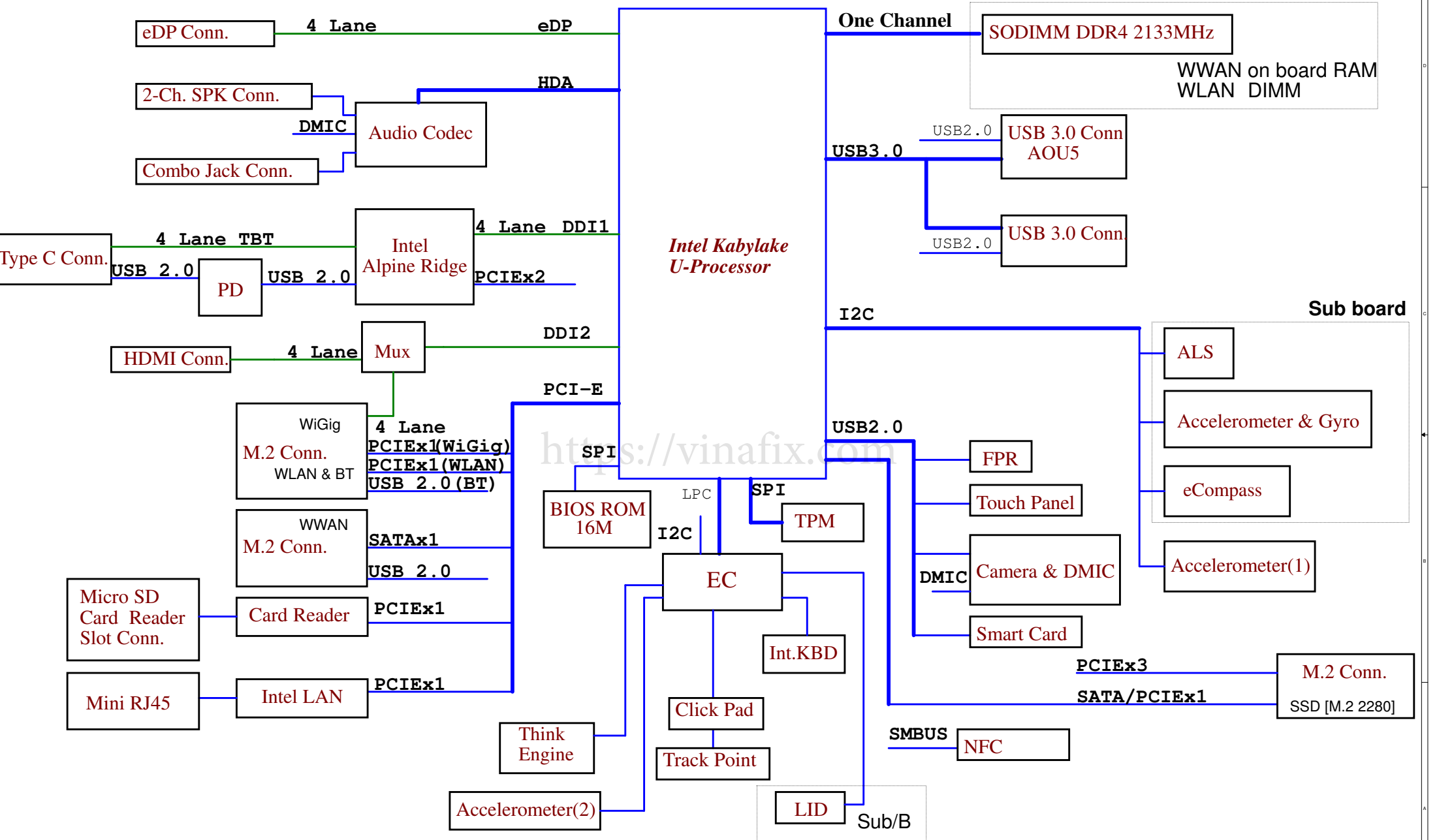


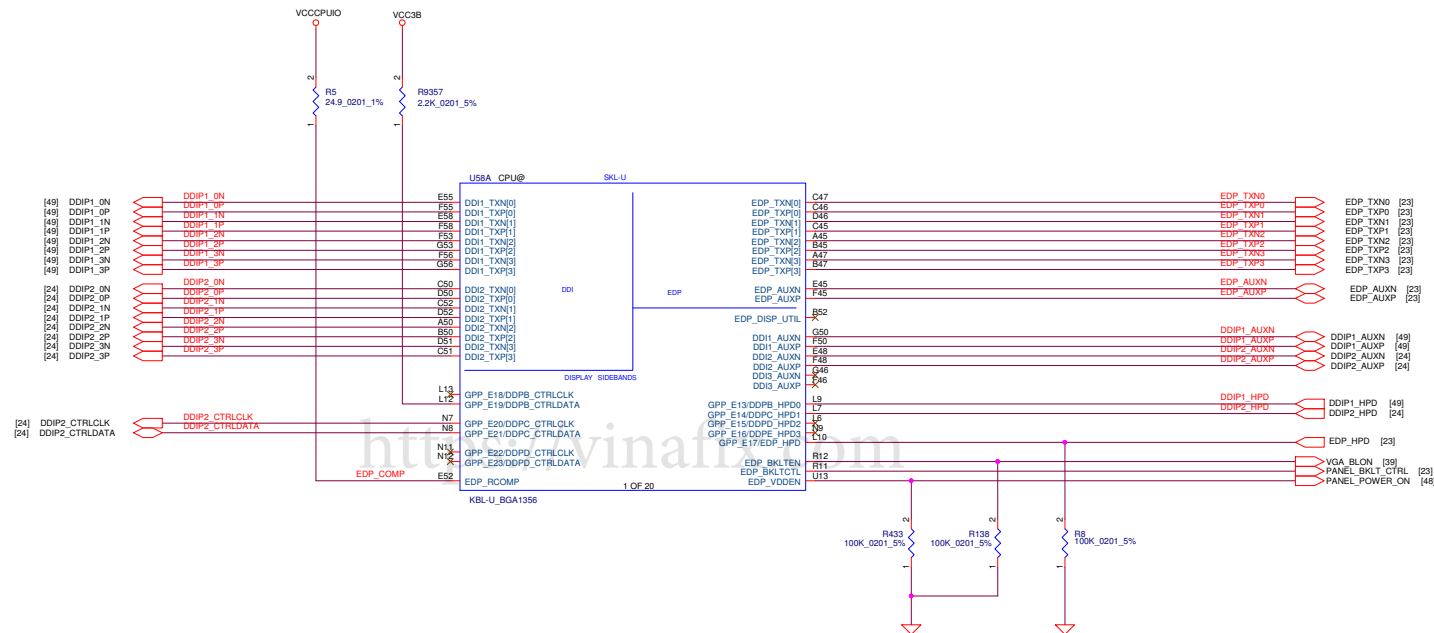
TABLE : Function Strap

DDPB_CTRLDATA

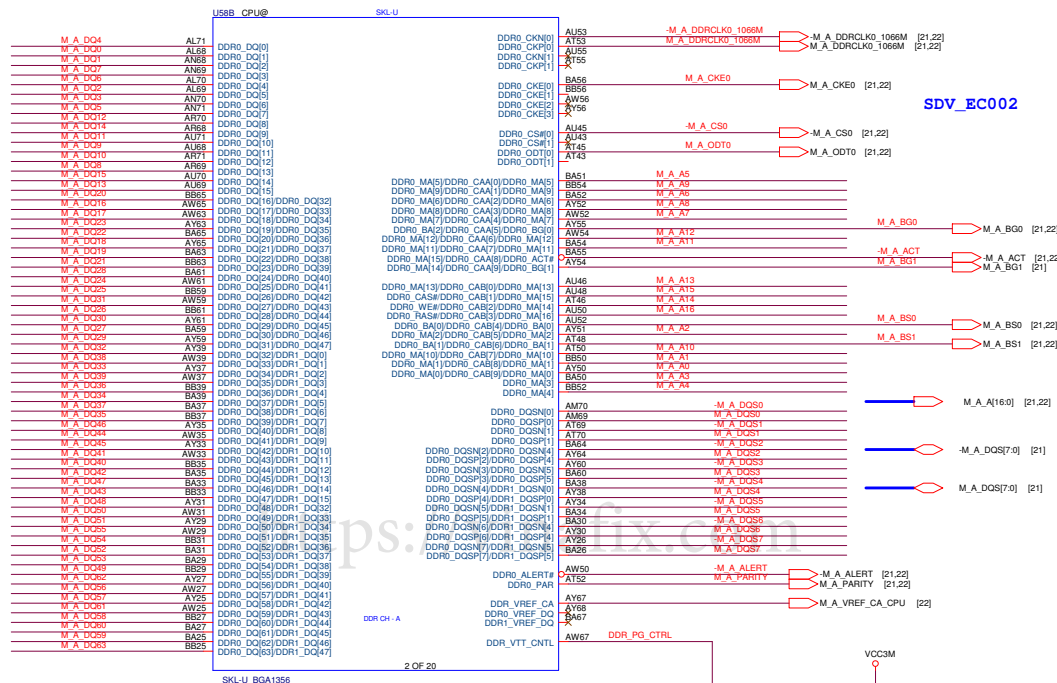
HIGH Port B is detected.
LOW Port B is not detected.

DDPC_CTRLDATA

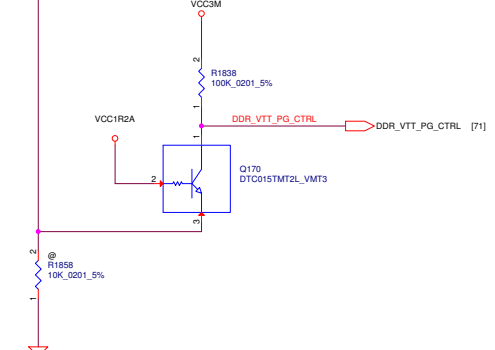
HIGH Port C is detected.
LOW Port C is not detected.



| | Pin | Interleave | Non-Interleave |
|---------|-------------|-------------|----------------|
| Block 0 | AL71 | DDRO_DQ[0] | DDRO_DQ[0] |
| | AL68 | DDRO_DQ[1] | DDRO_DQ[1] |
| | AN68 | DDRO_DQ[2] | DDRO_DQ[2] |
| | AN69 | DDRO_DQ[3] | DDRO_DQ[3] |
| | AL70 | DDRO_DQ[4] | DDRO_DQ[4] |
| | AL69 | DDRO_DQ[5] | DDRO_DQ[5] |
| | AN70 | DDRO_DQ[6] | DDRO_DQ[6] |
| | AN71 | DDRO_DQ[7] | DDRO_DQ[7] |
| | AR68 | DDRO_DQ[8] | DDRO_DQ[8] |
| | AR69 | DDRO_DQ[9] | DDRO_DQ[9] |
| | AU71 | DDRO_DQ[10] | DDRO_DQ[10] |
| | AU68 | DDRO_DQ[11] | DDRO_DQ[11] |
| | AR71 | DDRO_DQ[12] | DDRO_DQ[12] |
| | AR69 | DDRO_DQ[13] | DDRO_DQ[13] |
| AU70 | DDRO_DQ[14] | DDRO_DQ[14] | |
| AU69 | DDRO_DQ[15] | DDRO_DQ[15] | |
| Block 2 | BB65 | DDRO_DQ[16] | DDRO_DQ[32] |
| | AW65 | DDRO_DQ[17] | DDRO_DQ[33] |
| | AW63 | DDRO_DQ[18] | DDRO_DQ[34] |
| | AY63 | DDRO_DQ[19] | DDRO_DQ[35] |
| | BA65 | DDRO_DQ[20] | DDRO_DQ[36] |
| | AY65 | DDRO_DQ[21] | DDRO_DQ[37] |
| | BA63 | DDRO_DQ[22] | DDRO_DQ[38] |
| | BB63 | DDRO_DQ[23] | DDRO_DQ[39] |
| | BA61 | DDRO_DQ[24] | DDRO_DQ[40] |
| | AW61 | DDRO_DQ[25] | DDRO_DQ[41] |
| | BB59 | DDRO_DQ[26] | DDRO_DQ[42] |
| | AW59 | DDRO_DQ[27] | DDRO_DQ[43] |
| | BB61 | DDRO_DQ[28] | DDRO_DQ[44] |
| | AY61 | DDRO_DQ[29] | DDRO_DQ[45] |
| BA59 | DDRO_DQ[30] | DDRO_DQ[46] | |
| AY59 | DDRO_DQ[31] | DDRO_DQ[47] | |
| Block 4 | AY39 | DDRO_DQ[32] | DDRI_DQ[0] |
| | AW39 | DDRO_DQ[33] | DDRI_DQ[1] |
| | AY37 | DDRO_DQ[34] | DDRI_DQ[2] |
| | AW37 | DDRO_DQ[35] | DDRI_DQ[3] |
| | BB39 | DDRO_DQ[36] | DDRI_DQ[4] |
| | BA39 | DDRO_DQ[37] | DDRI_DQ[5] |
| | BA37 | DDRO_DQ[38] | DDRI_DQ[6] |
| | BB37 | DDRO_DQ[39] | DDRI_DQ[7] |
| | AY35 | DDRO_DQ[40] | DDRI_DQ[8] |
| | AW35 | DDRO_DQ[41] | DDRI_DQ[9] |
| | AY33 | DDRO_DQ[42] | DDRI_DQ[10] |
| | AW33 | DDRO_DQ[43] | DDRI_DQ[11] |
| | BB35 | DDRO_DQ[44] | DDRI_DQ[12] |
| | BA35 | DDRO_DQ[45] | DDRI_DQ[13] |
| BA33 | DDRO_DQ[46] | DDRI_DQ[14] | |
| BB33 | DDRO_DQ[47] | DDRI_DQ[15] | |
| Block 6 | AY31 | DDRO_DQ[48] | DDRI_DQ[32] |
| | AW31 | DDRO_DQ[49] | DDRI_DQ[33] |
| | AY29 | DDRO_DQ[50] | DDRI_DQ[34] |
| | AW29 | DDRO_DQ[51] | DDRI_DQ[35] |
| | BB31 | DDRO_DQ[52] | DDRI_DQ[36] |
| | BA31 | DDRO_DQ[53] | DDRI_DQ[37] |
| | BA29 | DDRO_DQ[54] | DDRI_DQ[38] |
| | BB29 | DDRO_DQ[55] | DDRI_DQ[39] |
| | AY27 | DDRO_DQ[56] | DDRI_DQ[40] |
| | AW27 | DDRO_DQ[57] | DDRI_DQ[41] |
| | AY25 | DDRO_DQ[58] | DDRI_DQ[42] |
| | AW25 | DDRO_DQ[59] | DDRI_DQ[43] |
| | BB27 | DDRO_DQ[60] | DDRI_DQ[44] |
| | BA27 | DDRO_DQ[61] | DDRI_DQ[45] |
| BA25 | DDRO_DQ[62] | DDRI_DQ[46] | |
| BB25 | DDRO_DQ[63] | DDRI_DQ[47] | |



| Pin | DDR3L | LPDDR3 | DDR4 |
|------|-------------|-------------|-------------|
| BA51 | DDRO_MA[5] | DDRO_CAA[0] | DDRO_MA[5] |
| B854 | DDRO_MA[9] | DDRO_CAA[1] | DDRO_MA[9] |
| BA52 | DDRO_MA[6] | DDRO_CAA[2] | DDRO_MA[6] |
| AY52 | DDRO_MA[8] | DDRO_CAA[3] | DDRO_MA[8] |
| AW52 | DDRO_MA[7] | DDRO_CAA[4] | DDRO_MA[7] |
| AY55 | DDRO_BA[2] | DDRO_CAA[5] | DDRO_BG[0] |
| AW54 | DDRO_MA[12] | DDRO_CAA[6] | DDRO_MA[12] |
| BA54 | DDRO_MA[11] | DDRO_CAA[7] | DDRO_MA[11] |
| BA55 | DDRO_MA[15] | DDRO_CAA[8] | DDRO_ACT# |
| AY54 | DDRO_MA[14] | DDRO_CAA[9] | DDRO_BG[1] |
| | | | |
| AU46 | DDRO_MA[13] | DDRO_CAB[0] | DDRO_MA[13] |
| AU48 | DDRO_CAS# | DDRO_CAB[1] | DDRO_MA[15] |
| AT46 | DDRO_MA[3] | DDRO_CAB[2] | DDRO_MA[3] |
| AU50 | DDRO_RAS# | DDRO_CAB[3] | DDRO_MA[16] |
| AU52 | DDRO_BA[0] | DDRO_CAB[4] | DDRO_BA[0] |
| AY51 | DDRO_MA[2] | DDRO_CAB[5] | DDRO_MA[2] |
| AT48 | DDRO_BA[1] | DDRO_CAB[6] | DDRO_BA[1] |
| AT50 | DDRO_MA[10] | DDRO_CAB[7] | DDRO_MA[10] |
| B850 | DDRO_MA[1] | DDRO_CAB[8] | DDRO_MA[1] |
| BY50 | DDRO_MA[0] | DDRO_CAB[9] | DDRO_MA[0] |
| BA50 | DDRO_MA[3] | Not Used | DDRO_MA[3] |
| B852 | DDRO_MA[4] | Not Used | DDRO_MA[4] |



1

15310

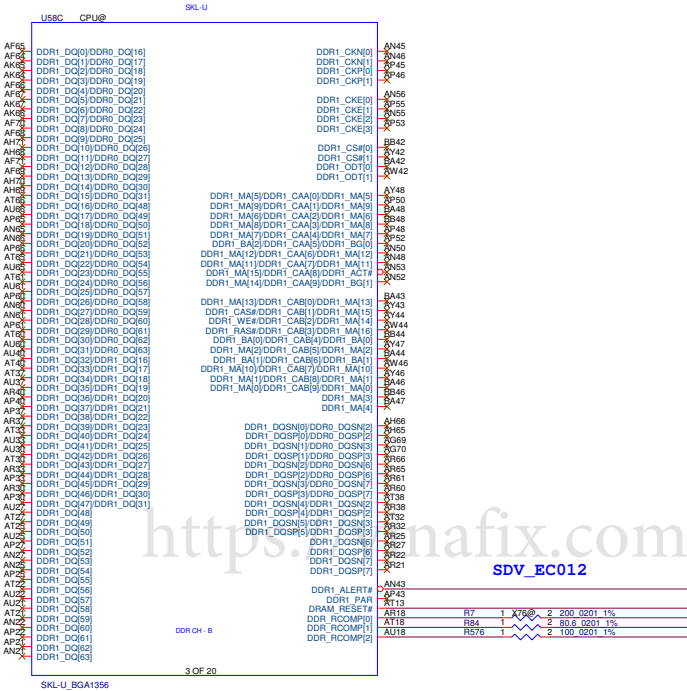
| | Pin | Interleave | Non-Interleave |
|---------|------|---------------|----------------|
| Block 0 | AM70 | DDR0_DQSIN[0] | DDR0_DQSIN[0] |
| | AM69 | DDR0_DQSIN[1] | DDR0_DQSP0[0] |
| | AT69 | DDR0_DQSIN[1] | DDR0_DQSIN[1] |
| | AT70 | DDR0_DQSP[1] | DDR0_DQSP[1] |
| Block 2 | BA64 | DDR0_DQSIN[2] | DDR0_DQSIN[4] |
| | AV64 | DDR0_DQSP[2] | DDR0_DQSP[4] |
| | AV60 | DDR0_DQSIN[3] | DDR0_DQSIN[5] |
| | BA60 | DDR0_DQSP[3] | DDR0_DQSP[5] |
| Block 4 | BA38 | DDR0_DQSIN[4] | DDR0_DQSIN[0] |
| | AV38 | DDR0_DQSP[4] | DDR0_DQSP[0] |
| | AY34 | DDR0_DQSIN[5] | DDR1_DQSIN[1] |
| | BA34 | DDR0_DQSP[5] | DDR1_DQSP[1] |
| Block 6 | BA30 | DDR0_DQSIN[6] | DDR1_DQSIN[4] |
| | AY30 | DDR0_DQSP[6] | DDR1_DQSP[4] |
| | AY26 | DDR0_DQSIN[7] | DDR1_DQSIN[5] |
| | BA26 | DDR0_DQSP[7] | DDR1_DQSP[5] |

| | | | | | | | | |
|---|--------------------|-----------------|------------|--|---------|-----------------------|---------------------------|----------|
| Security Classification | Compul Secret Data | | | | Title | | Compul Electronics, Inc. | |
| | 2014/11/04 | Deciphered Date | 2016/12/31 | | | | CPU(2/16) : DDR CHANNEL-A | |
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| | | | | | Date | LA-E292P | 1.0 | |
| | | | | | Created | Tuesday, May 03, 2016 | Sheet | 4 of 102 |

TABLE

| | Pin | Interleave | Non-Interleave |
|---------|------|-------------|----------------|
| Block 1 | AF65 | DDR1_DQ[0] | DDR0_DQ[16] |
| | AF64 | DDR1_DQ[1] | DDR0_DQ[17] |
| | AK65 | DDR1_DQ[2] | DDR0_DQ[18] |
| | AK64 | DDR1_DQ[3] | DDR0_DQ[19] |
| | AF66 | DDR1_DQ[4] | DDR0_DQ[20] |
| | AF67 | DDR1_DQ[5] | DDR0_DQ[21] |
| | AK67 | DDR1_DQ[6] | DDR0_DQ[22] |
| | AK66 | DDR1_DQ[7] | DDR0_DQ[23] |
| | AF70 | DDR1_DQ[8] | DDR0_DQ[24] |
| | AF68 | DDR1_DQ[9] | DDR0_DQ[25] |
| | AH71 | DDR1_DQ[10] | DDR0_DQ[26] |
| | AH68 | DDR1_DQ[11] | DDR0_DQ[27] |
| | AF71 | DDR1_DQ[12] | DDR0_DQ[28] |
| | AH70 | DDR1_DQ[13] | DDR0_DQ[29] |
| | AF69 | DDR1_DQ[14] | DDR0_DQ[30] |
| | AH69 | DDR1_DQ[15] | DDR0_DQ[31] |
| Block 3 | AT66 | DDR1_DQ[16] | DDR0_DQ[48] |
| | AU66 | DDR1_DQ[17] | DDR0_DQ[49] |
| | AP65 | DDR1_DQ[18] | DDR0_DQ[50] |
| | AN65 | DDR1_DQ[19] | DDR0_DQ[51] |
| | AN66 | DDR1_DQ[20] | DDR0_DQ[52] |
| | AP66 | DDR1_DQ[21] | DDR0_DQ[53] |
| | AT65 | DDR1_DQ[22] | DDR0_DQ[54] |
| | AU65 | DDR1_DQ[23] | DDR0_DQ[55] |
| | AT61 | DDR1_DQ[24] | DDR0_DQ[56] |
| | AU61 | DDR1_DQ[25] | DDR0_DQ[57] |
| | AP60 | DDR1_DQ[26] | DDR0_DQ[58] |
| | AN60 | DDR1_DQ[27] | DDR0_DQ[59] |
| | AN61 | DDR1_DQ[28] | DDR0_DQ[60] |
| | AP61 | DDR1_DQ[29] | DDR0_DQ[61] |
| | AT60 | DDR1_DQ[30] | DDR0_DQ[62] |
| | AU60 | DDR1_DQ[31] | DDR0_DQ[63] |
| Block 5 | AU40 | DDR1_DQ[32] | DDR1_DQ[16] |
| | AT40 | DDR1_DQ[33] | DDR1_DQ[17] |
| | AT37 | DDR1_DQ[34] | DDR1_DQ[18] |
| | AU37 | DDR1_DQ[35] | DDR1_DQ[19] |
| | AR40 | DDR1_DQ[36] | DDR1_DQ[20] |
| | AP40 | DDR1_DQ[37] | DDR1_DQ[21] |
| | AP37 | DDR1_DQ[38] | DDR1_DQ[22] |
| | AR37 | DDR1_DQ[39] | DDR1_DQ[23] |
| | AT33 | DDR1_DQ[40] | DDR1_DQ[24] |
| | AU33 | DDR1_DQ[41] | DDR1_DQ[25] |
| | AU30 | DDR1_DQ[42] | DDR1_DQ[26] |
| | AT30 | DDR1_DQ[43] | DDR1_DQ[27] |
| | AR33 | DDR1_DQ[44] | DDR1_DQ[28] |
| | AP33 | DDR1_DQ[45] | DDR1_DQ[29] |
| | AR30 | DDR1_DQ[46] | DDR1_DQ[30] |
| | AP30 | DDR1_DQ[47] | DDR1_DQ[31] |
| Block 7 | AU27 | DDR1_DQ[48] | DDR1_DQ[48] |
| | AT27 | DDR1_DQ[49] | DDR1_DQ[49] |
| | AT25 | DDR1_DQ[50] | DDR1_DQ[50] |
| | AU25 | DDR1_DQ[51] | DDR1_DQ[51] |
| | AP27 | DDR1_DQ[52] | DDR1_DQ[52] |
| | AN27 | DDR1_DQ[53] | DDR1_DQ[53] |
| | AN25 | DDR1_DQ[54] | DDR1_DQ[54] |
| | AP25 | DDR1_DQ[55] | DDR1_DQ[55] |
| | AT22 | DDR1_DQ[56] | DDR1_DQ[56] |
| | AU22 | DDR1_DQ[57] | DDR1_DQ[57] |
| | AU21 | DDR1_DQ[58] | DDR1_DQ[58] |
| | AT21 | DDR1_DQ[59] | DDR1_DQ[59] |
| | AN22 | DDR1_DQ[60] | DDR1_DQ[60] |
| | AP22 | DDR1_DQ[61] | DDR1_DQ[61] |
| | AP21 | DDR1_DQ[62] | DDR1_DQ[62] |
| | AN21 | DDR1_DQ[63] | DDR1_DQ[63] |

LOGIC



| | Pin | Interleave | Non-Interleave |
|---------|------|--------------|----------------|
| Block 1 | AH66 | DDR1_DQSN[0] | DDR0_DQSN[2] |
| | AH65 | DDR1_DQSP[0] | DDR0_DQSP[2] |
| | AG69 | DDR1_DQSN[1] | DDR0_DQSN[3] |
| Block 3 | AR66 | DDR1_DQSN[2] | DDR0_DQSN[4] |
| | AR65 | DDR1_DQSP[2] | DDR0_DQSP[4] |
| | AR61 | DDR1_DQSN[3] | DDR0_DQSN[5] |
| | AR60 | DDR1_DQSP[3] | DDR0_DQSP[5] |
| Block 5 | AT38 | DDR1_DQSN[4] | DDR1_DQSN[2] |
| | AT37 | DDR1_DQSP[4] | DDR1_DQSP[2] |
| | AT32 | DDR1_DQSN[5] | DDR1_DQSN[3] |
| | AR32 | DDR1_DQSP[5] | DDR1_DQSP[3] |
| Block 7 | AR25 | DDR1_DQSN[6] | DDR1_DQSN[6] |
| | AR27 | DDR1_DQSP[6] | DDR1_DQSP[6] |
| | AR22 | DDR1_DQSN[7] | DDR1_DQSN[7] |
| | AR21 | DDR1_DQSP[7] | DDR1_DQSP[7] |

LOGIC

TABLE

| Pin | DDR3L | LPDDR3 | DDR4 |
|------|-------------|-------------|-------------|
| AY48 | DDR1_MA[5] | DDR1_CAA[0] | DDR1_MA[5] |
| AP50 | DDR1_MA[9] | DDR1_CAA[1] | DDR1_MA[9] |
| BA48 | DDR1_MA[6] | DDR1_CAA[2] | DDR1_MA[6] |
| BB48 | DDR1_MA[8] | DDR1_CAA[3] | DDR1_MA[8] |
| AP48 | DDR1_MA[7] | DDR1_CAA[4] | DDR1_MA[7] |
| AP52 | DDR1_BA[2] | DDR1_CAA[5] | DDR1_BG[0] |
| AN50 | DDR1_MA[12] | DDR1_CAA[6] | DDR1_MA[12] |
| AN48 | DDR1_MA[11] | DDR1_CAA[7] | DDR1_MA[11] |
| AN53 | DDR1_MA[15] | DDR1_CAA[8] | DDR1_ACT[7] |
| AN52 | DDR1_MA[14] | DDR1_CAA[9] | DDR1_BG[1] |
| | | | |
| BA43 | DDR1_MA[13] | DDR1_CAB[0] | DDR1_MA[13] |
| AY43 | DDR1_CAS# | DDR1_CAB[1] | DDR1_MA[15] |
| AY44 | DDR1_VEH# | DDR1_CAB[2] | DDR1_MA[14] |
| AW44 | DDR1_RAS# | DDR1_CAB[3] | DDR1_MA[16] |
| BB44 | DDR1_BA[0] | DDR1_CAB[4] | DDR1_BA[0] |
| AY47 | DDR1_MA[2] | DDR1_CAB[5] | DDR1_MA[2] |
| BA44 | DDR1_BA[1] | DDR1_CAB[6] | DDR1_BA[1] |
| AW46 | DDR1_MA[10] | DDR1_CAB[7] | DDR1_MA[10] |
| AY46 | DDR1_MA[1] | DDR1_CAB[8] | DDR1_MA[1] |
| BA46 | DDR1_MA[0] | DDR1_CAB[9] | DDR1_MA[0] |
| BB46 | DDR1_MA[3] | Not Used | DDR1_MA[3] |
| BA47 | DDR1_MA[4] | Not Used | DDR1_MA[4] |

LOGIC

| | SDP | DDP |
|----|--------|--------|
| R7 | 200 1% | 121 1% |

| SPI0_MOSI (Boot Halt) | |
|-----------------------|--------------------|
| HIGH | Disabled (Default) |
| LOW | Enabled |

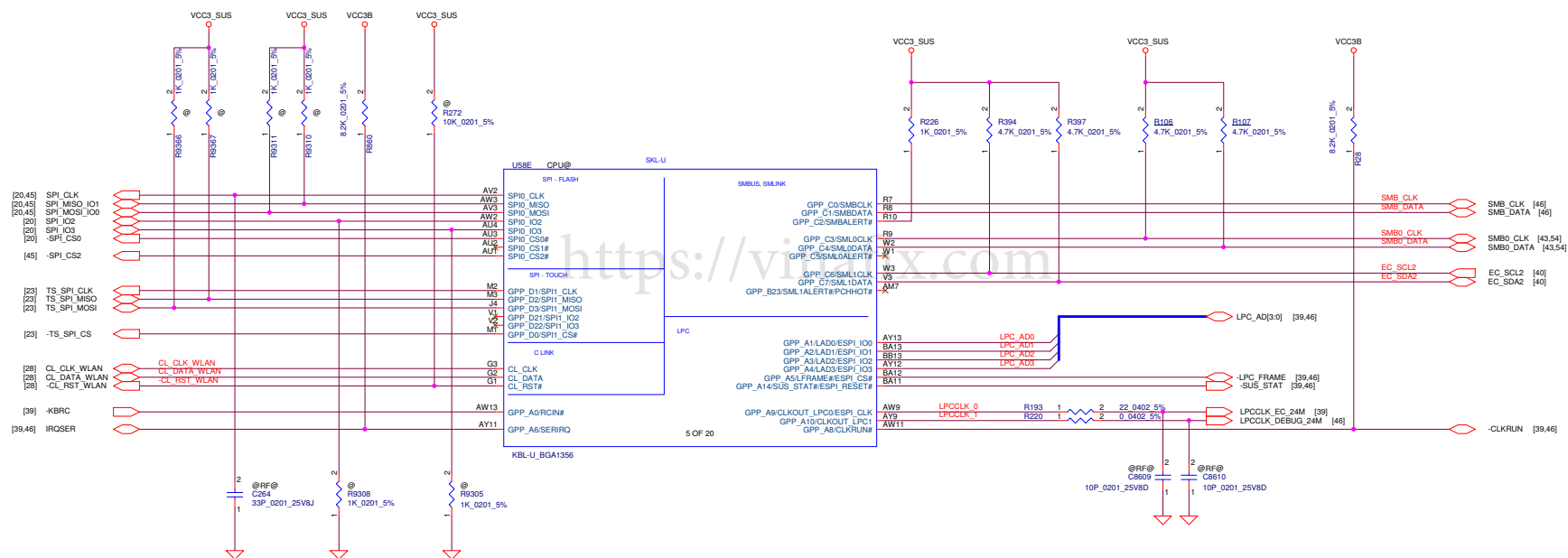
| SPI0_MISO (JTAG ODT Diabler) | |
|------------------------------|-------------------|
| HIGH | Enabled (Default) |
| LOW | Disabled |

| GPP_C5/SML0ALERT # (LPC or eSPI) | |
|----------------------------------|---------------------------|
| HIGH | eSPI is selected |
| LOW | LPC is selected (Default) |

← LOGIC

| GPP_C2/SMBALERT# (TLS Confidentiality) | |
|--|---|
| HIGH | Enable ME Crypto TLS with Confidentiality |
| LOW | Disable ME Crypto TLS (Default) |

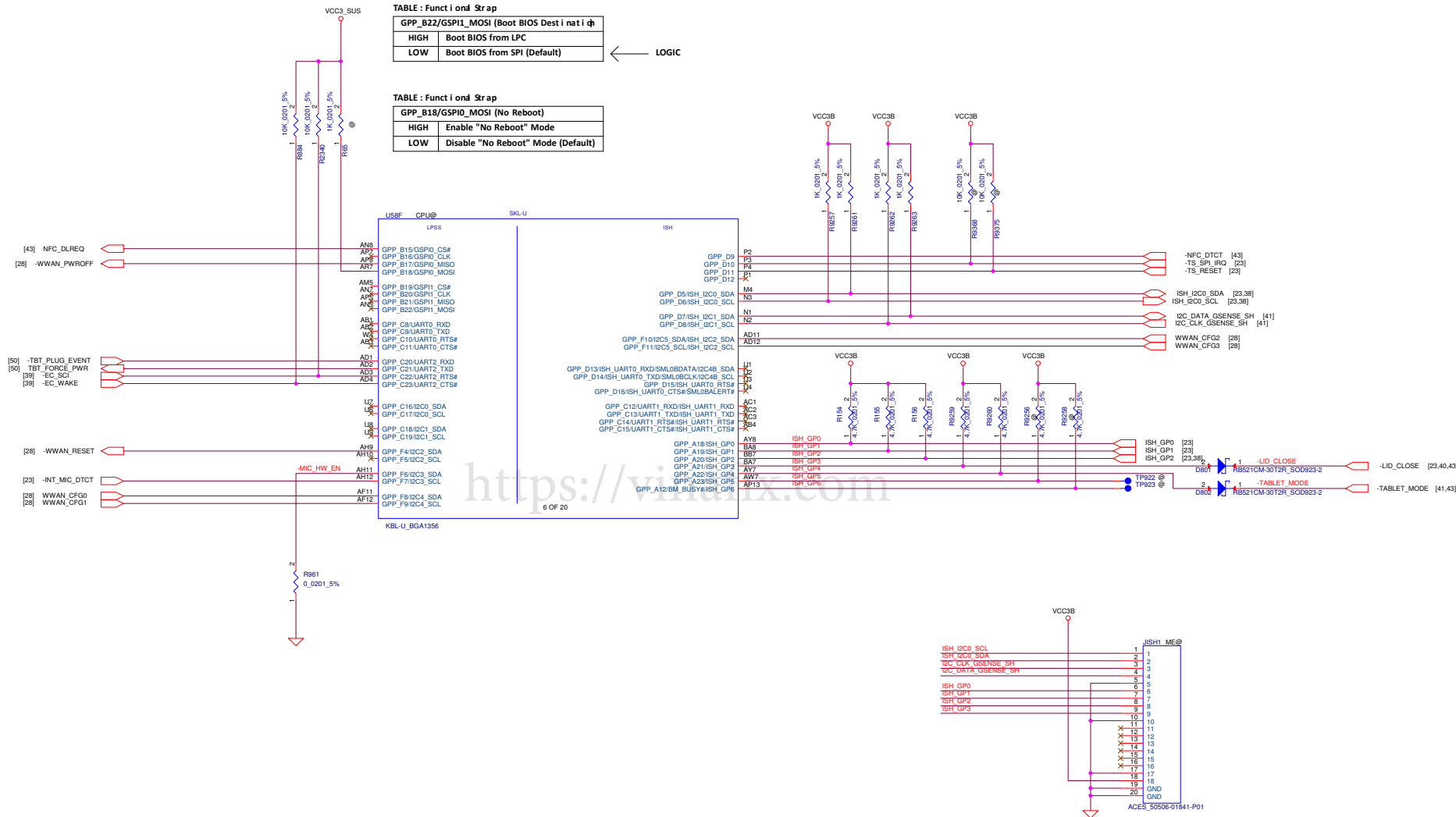
← LOGIC

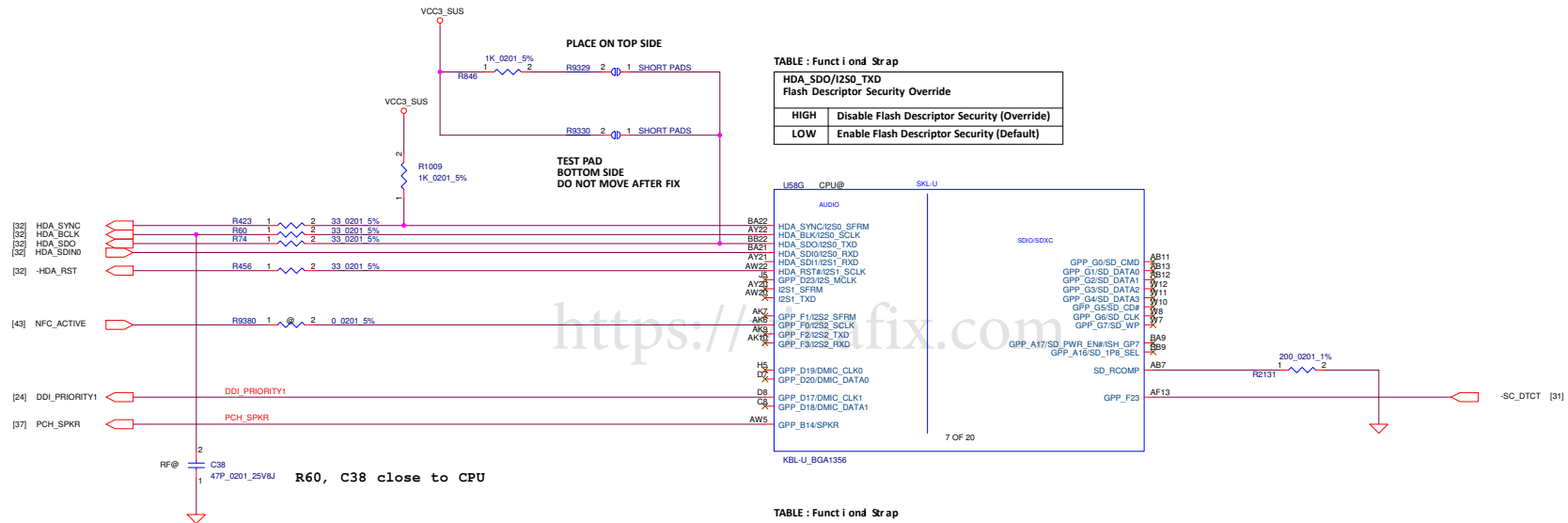


| SPI0_IO2 (Consent Strap) | |
|--------------------------|-------------------|
| HIGH | Enabled (Default) |
| LOW | Disabled |

| SPI0_IO3 (A0 Personality Strap) | |
|---------------------------------|--------------------|
| HIGH | Disabled (Default) |
| LOW | Enabled |

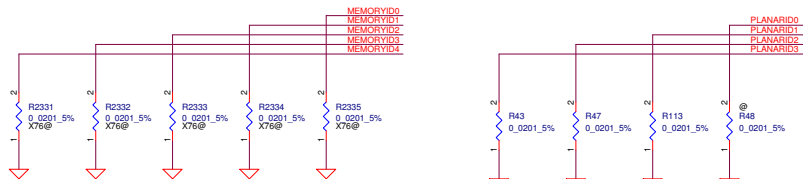
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|---|------------|--------------------|------------|--|--|
| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | Compal Electronics, Inc. CPU(516) : LPC/SPI/SMBUS/C-LINK | |
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TABLE

| MEMORY[4..0] | U125, U126, U127, U128 | | R7 (Rcomp0) |
|--------------|-----------------------------|--------------------|-------------|
| 00110B | Samsung K4A8G16SWB-BCRC | 8Gbit SDP | 4GB |
| 00111B | Micron MT40A512M16JY-083E:B | 8Gbit SDP | 4GB |
| 01000B | Micron MT40A1G16WBU-083E:B | 16Gbit DDP | 8GB |
| 01001B | Hynix H5AN8G6NAFR-UHC | 8Gbit SDP | 4GB |
| 01010B | Hynix T80 | 16Gbit DDP | 8GB |
| 01011B | Samsung K4AAG16SWB-MCRC | 16Gbit DDP | 8GB |
| 11111B | NO_ASM | No Soldered Memory | |



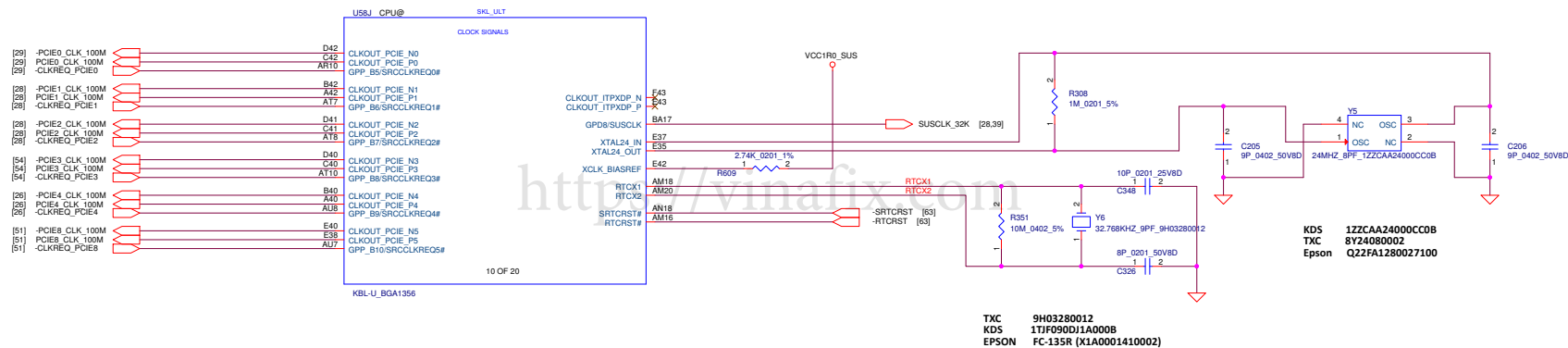
TABLE

| LEVEL | PLANAR ID | | | |
|-------|-----------|-----|------|-----|
| | 3 | 2 | 1 | 0 |
| | R43 | R47 | R113 | R48 |
| 1 | NA | NA | NA | NA |
| 0 | ASM | ASM | ASM | ASM |

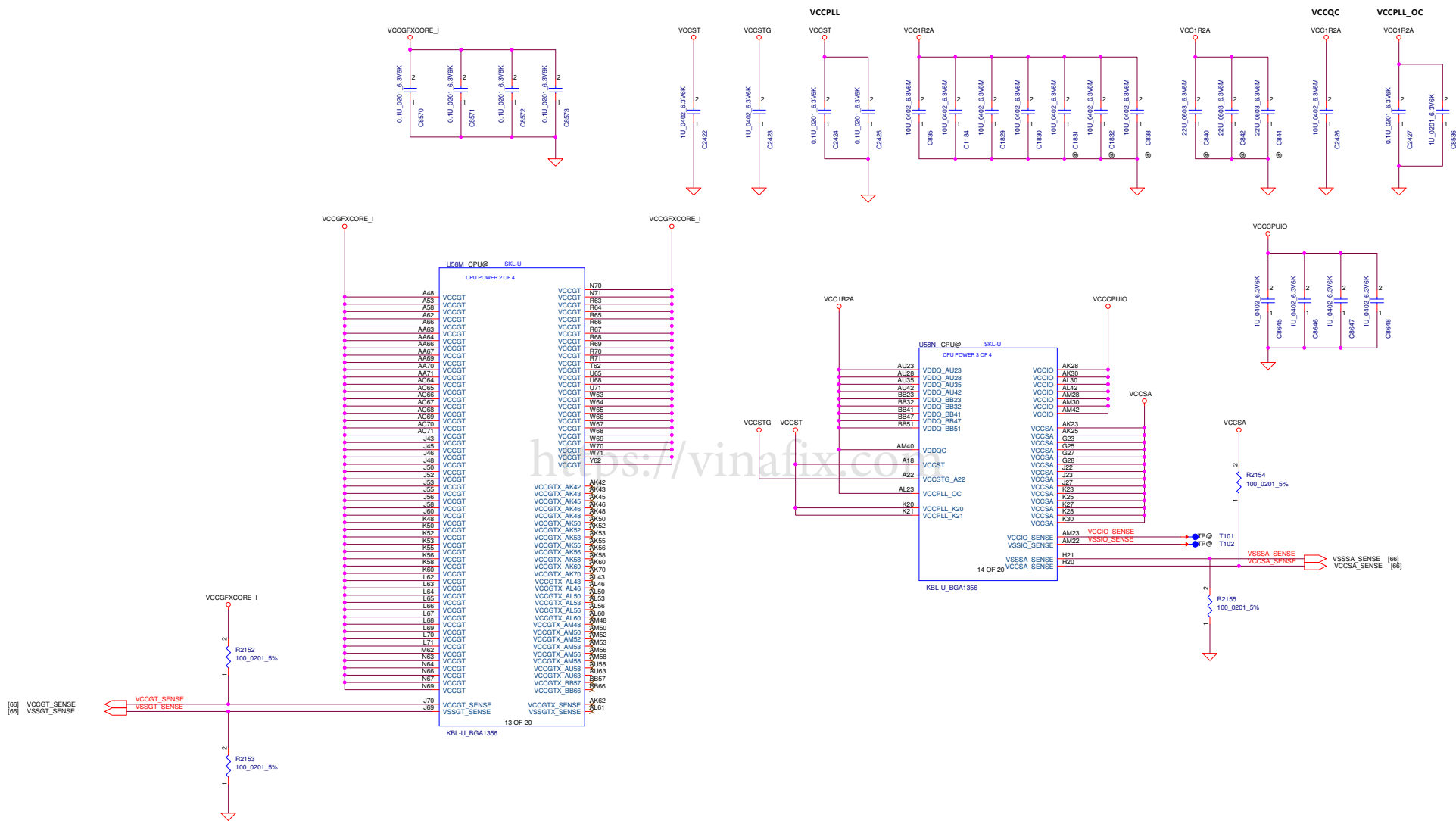
TABLE

| LEVEL | PLANARID[3..0] |
|-------|----------------|
| SDV | 0001B |
| FVT | 0010B |
| SIT | 0011B |
| SIT-R | 0100B |
| SVT | 0101B |

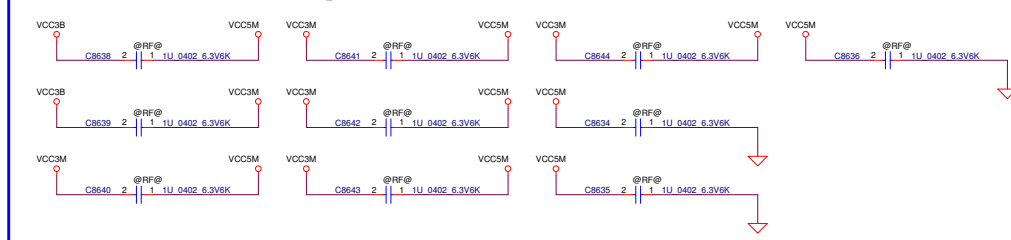
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|---|--------------------|-----------------|--------------------------|------------------|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | Title |
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| Size | Document | Number | Rev | 0.5 |
| Custom | LA-E292P | Date | Tuesday, May 03, 2016 | Sheet 11 of 75 |



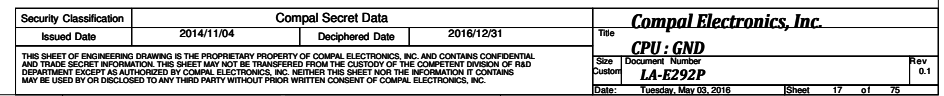
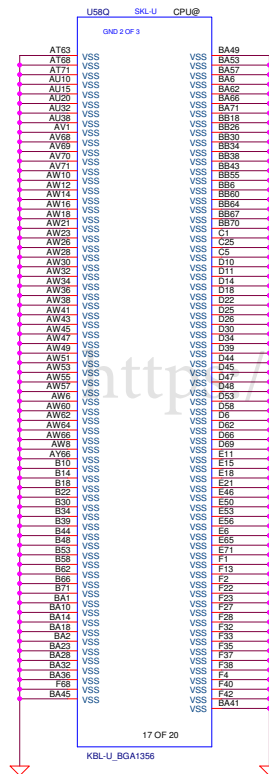
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| | | Size | | Document Number | |
| | | | | LA-E292P | |
| | | Date | | Tuesday, May 03, 2016 | |
| | | Sheet | | 12 of 75 | |
| | | | | Rev | |
| | | | | 0.1 | |



For RF cross moat capacitors

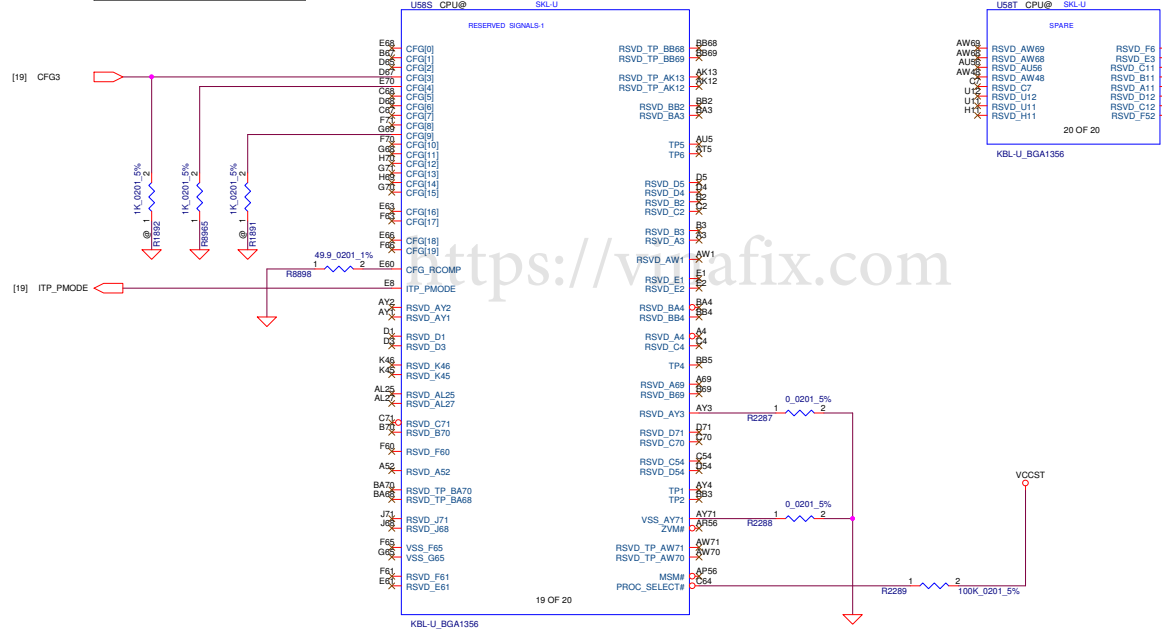


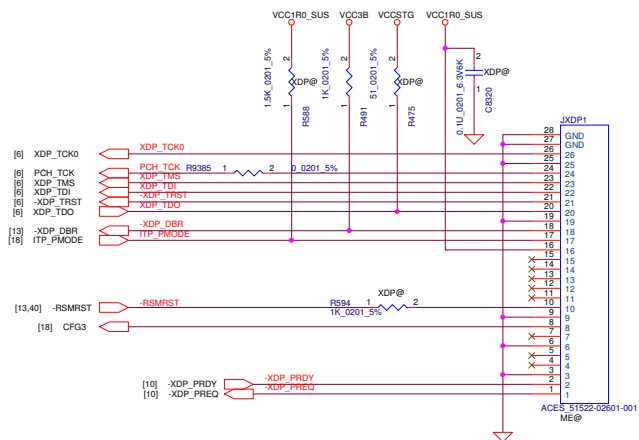
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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | Title | CPU : PCH POWER |
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| | | | | Document Number | LA-E292P |
| | | | | Rev | 0.1 |
| | | | | Date | Tuesday, May 03, 2016 |
| | | | | Sheet | 16 of 75 |



TABLE

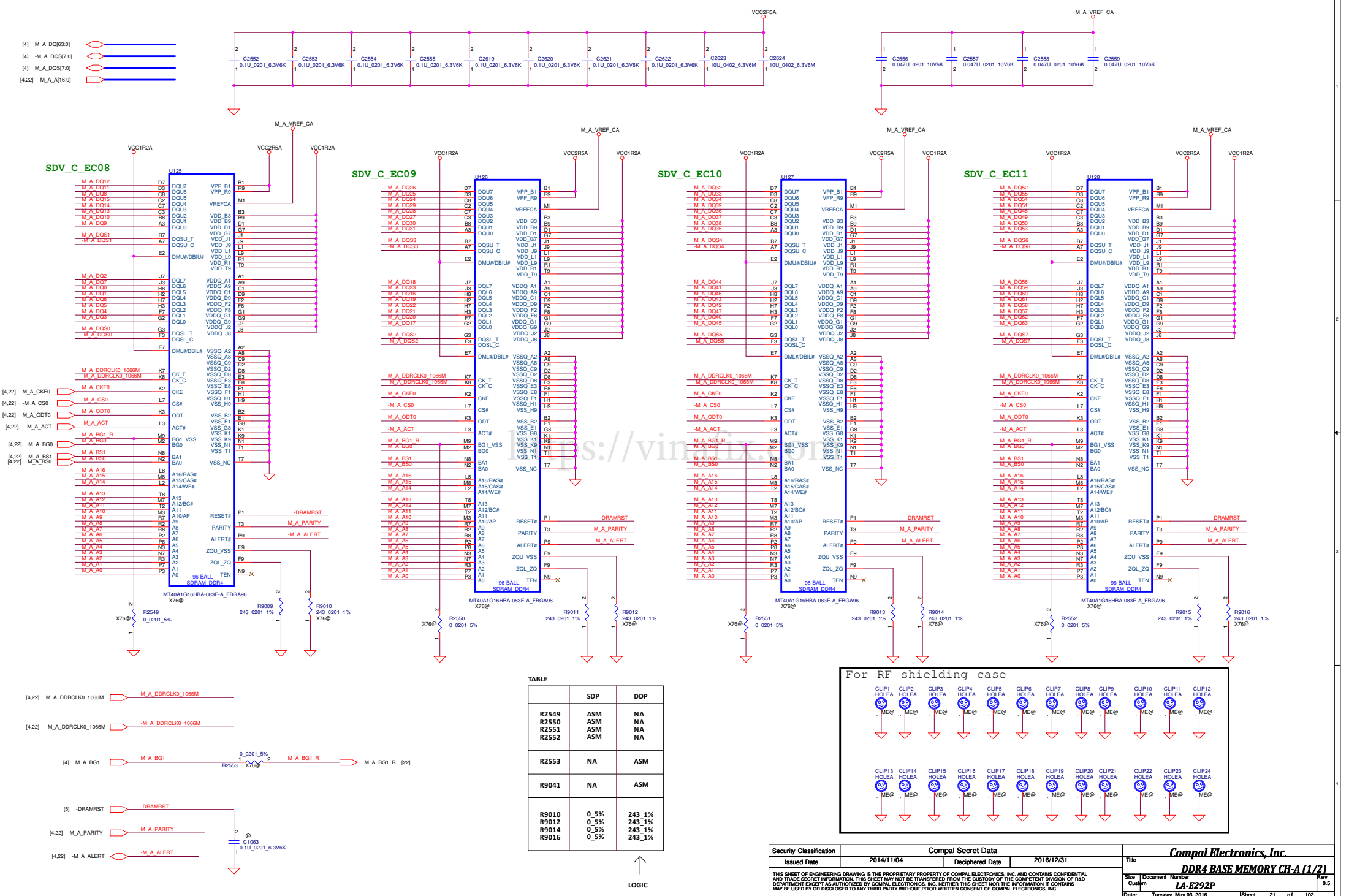
| |
|---|
| CFG0 : Stall Reset Sequence after PCU PLL Lock until deasserted 1 : No Stall 0 : Stall |
| CFG3 : MSR Privacy Bit Feature 1 : MSR (C80h) bit[0] set t i n 0 : MSR (C80h) bit[0] overridden |
| CFG4 : eDP Enable 1 : Disabled 0 : Enabled |
| CFG9 : SVID Bus Communicat i on 1 : Enabled 0 : Disabled |



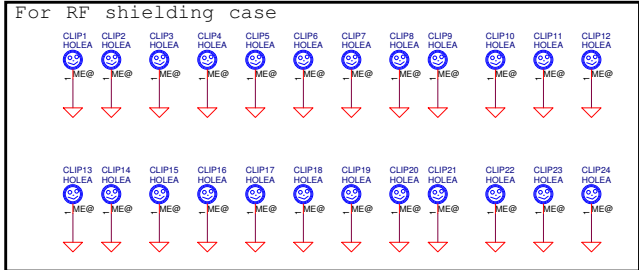


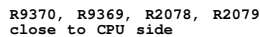
TABLE

| Logic | Ref Des | Merged | DCI 2.0 |
|---------|---------|--------|---------|
| Page 7 | R2559 | ASM | NO_ASM |
| Page 18 | R1982 | ASM | NO_ASM |
| Page 19 | J8 | ASM | NO_ASM |
| | C8320 | ASM | NO_ASM |
| | R475 | ASM | ASM |
| | R491 | ASM | ASM |
| | R588 | ASM | NO_ASM |
| | R594 | ASM | NO_ASM |
| | R2494 | ASM | NO_ASM |



| TABLE | | | |
|---------------------------|------|--------|-------|
| | SDP | DDP | |
| [4.22] M_A_DDRCLK0_1066M | ASM | NA | R2549 |
| | ASM | NA | |
| | ASM | NA | |
| [4.22] -M_A_DDRCLK0_1066M | NA | ASM | R2553 |
| | NA | ASM | |
| | NA | ASM | |
| [4] M_A_BG1 | NA | ASM | R9041 |
| | 0_5% | 243_1% | |
| | 0_5% | 243_1% | |
| | 0_5% | 243_1% | |





| | | | | | |
|---|------------|--------------------|------------|--|----------|
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| | | | | Document Number | 0.1 |
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| 2014/11/04 | | 2016/12/31 | | 2016/12/31 | |
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| Customer | | Number | | 0.5 | |
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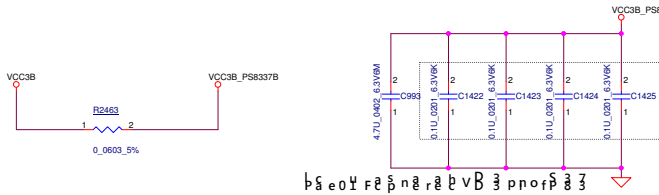
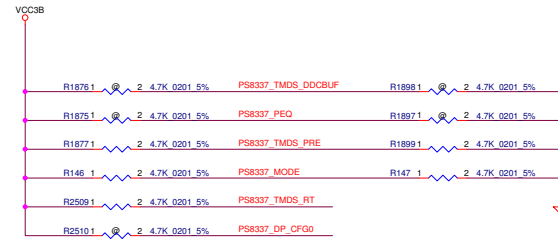


TABLE : Automatic Switching Mode (MODE = H, M)

| SW (DDI_PRIORITY1) |
|---|
| L DP Port has higher priority when both ports are plugged |
| H TMDs Port has higher priority when both ports are plugged |



| TMDs DDCBUF (INT PD) | R1876 | R1898 |
|-------------------------|--------|--------|
| DDC Active Buffer | ASM | NO_ASM |
| DDC Pass Through w/ PU | ASM | ASM |
| DDC Pass Through w/o PU | NO_ASM | NO_ASM |

LOGIC

| PEQ (INT PD) | R1875 | R1897 |
|--------------|--------|--------|
| HEQ 15dB | ASM | NO_ASM |
| LLEQ 5dB | ASM | ASM |
| LEQ 12dB | NO_ASM | NO_ASM |

LOGIC

| TMDs PRE (INT PD) | R1877 | R1899 |
|-------------------|--------|--------|
| 1.5dB | ASM | NO_ASM |
| 3.0dB | ASM | ASM |
| 0dB | NO_ASM | NO_ASM |

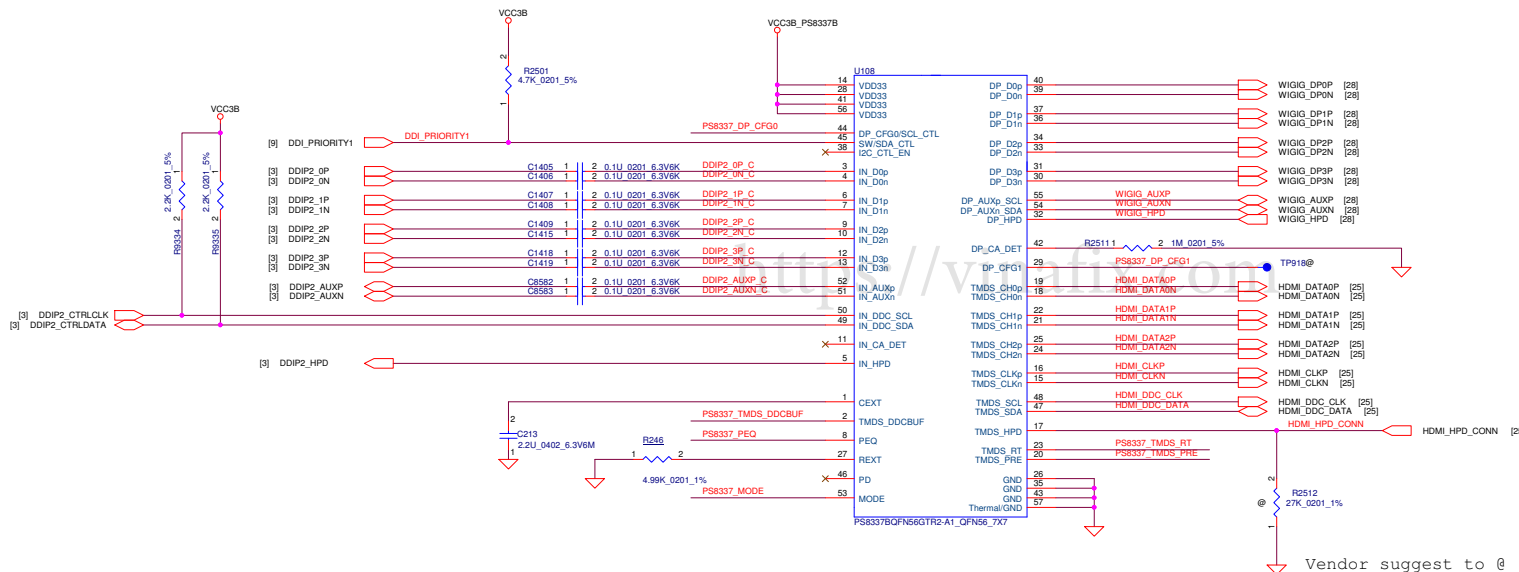
LOGIC

| MODE (INT PD) | R146 | R147 |
|-------------------------|--------|--------|
| Auto HDMI ID disable | ASM | NO_ASM |
| Auto HDMI ID enable | ASM | ASM |
| Control HDMI ID disable | NO_ASM | NO_ASM |

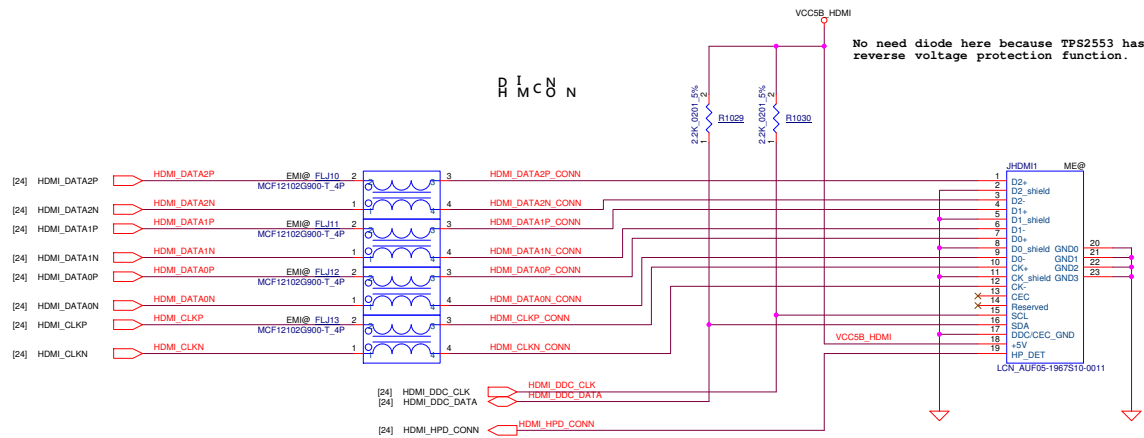
LOGIC

| TMDs RT (INT PD) | R2509 |
|-------------------|--------|
| OD w/ termination | ASM |
| OD | NO_ASM |

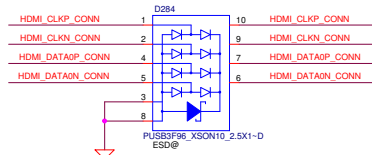
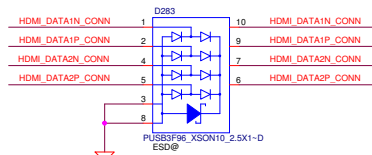
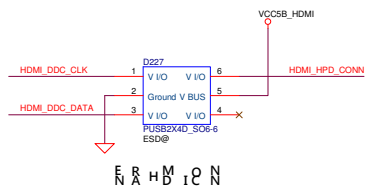
LOGIC



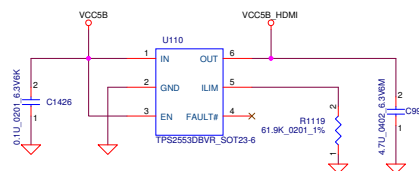
Vendor suggest to @



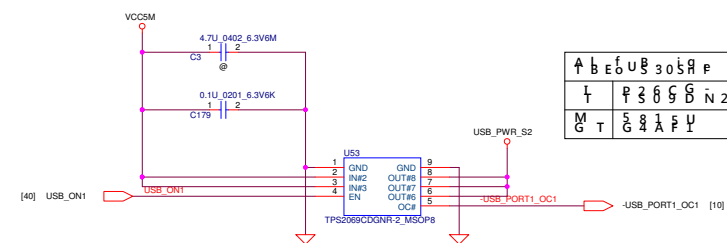
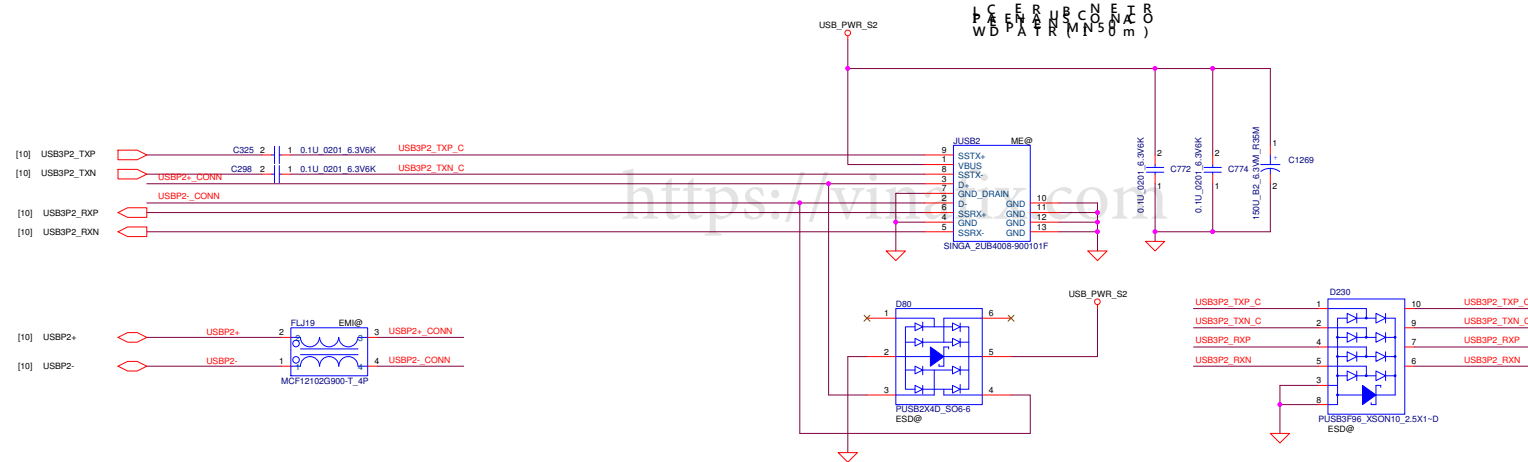
<https://vinafix.com>



Current Limit Target : 400mA
Requirement : 300mA
HDMI Spec : 50mA - 500mA



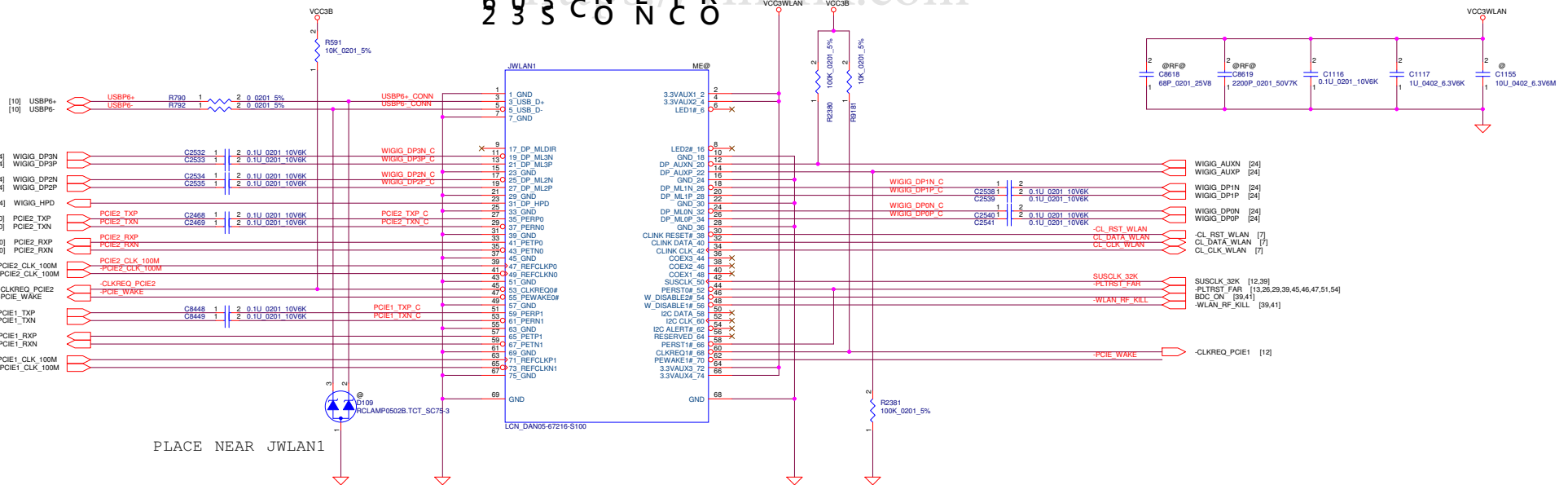
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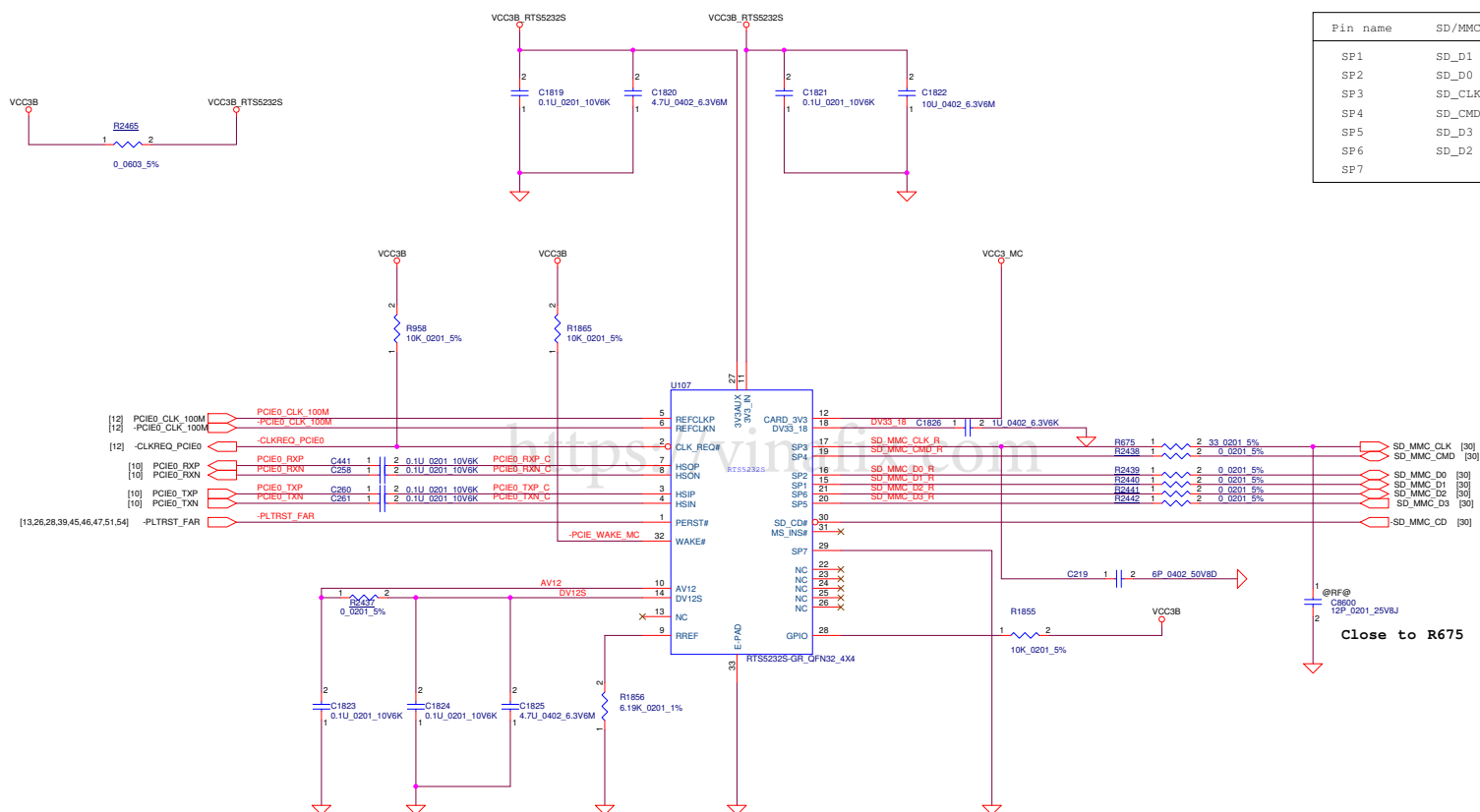
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|---|---|---|---|---|---|---|---|---|---|---|
| A | B | E | O | U | B | 3 | 0 | 5 | 9 | F |
| I | | P | 3 | 6 | 9 | G | D | N | 2 | |
| M | G | T | | 5 | 8 | 1 | A | F | U | |

| | | | | | | | |
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D F R O L W N A / B μ t o t / W G g
 6 9 3 C O N T R VCC3WLAN VCC3B

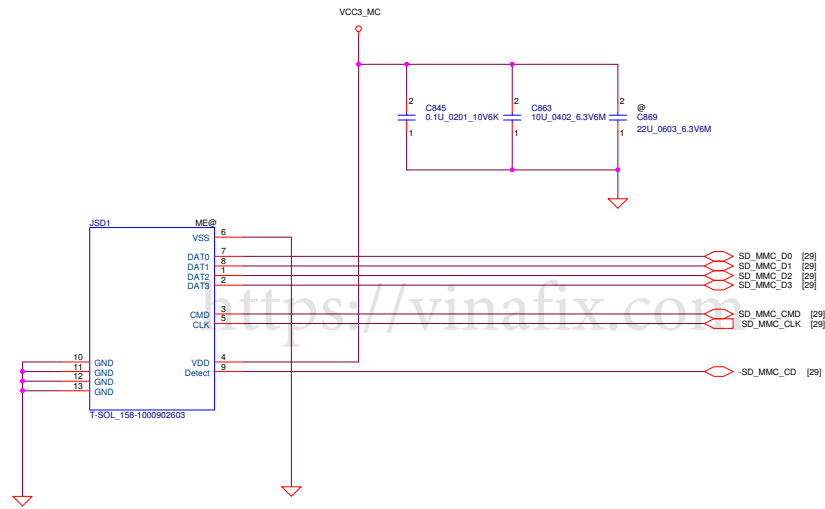


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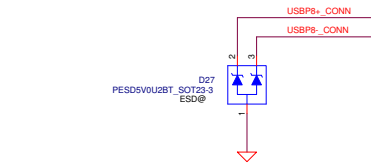
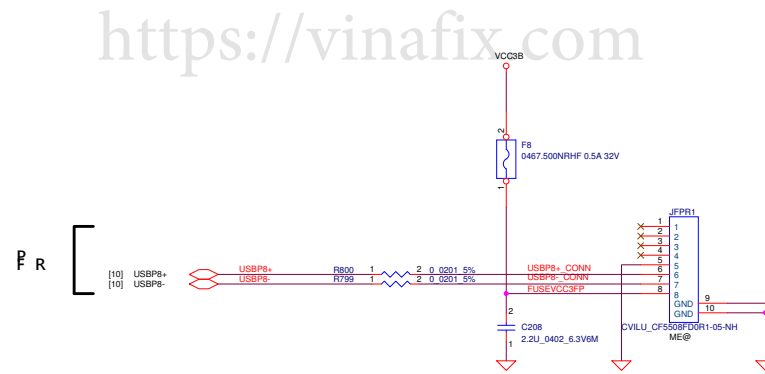
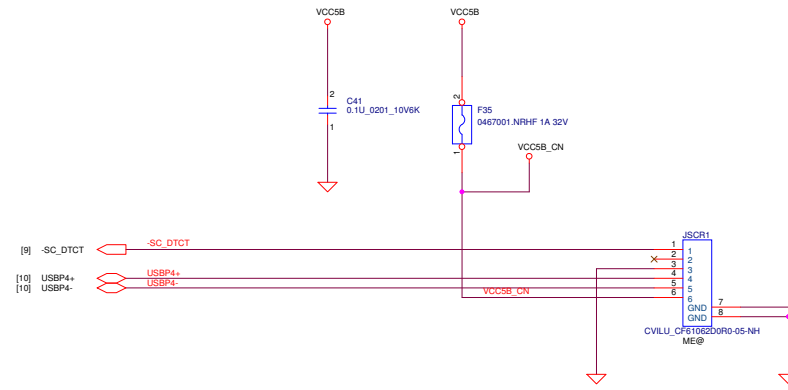


TABLE

| Pin name | SD/MMC | MEMORSTICK |
|----------|--------|------------|
| SP1 | SD_D1 | |
| SP2 | SD_D0 | MS_D1 |
| SP3 | SD_CLK | MS_D0 |
| SP4 | SD_CMD | MS_D2 |
| SP5 | SD_D3 | MS_D3 |
| SP6 | SD_D2 | MS_CLK |
| SP7 | | |



| | | | | | |
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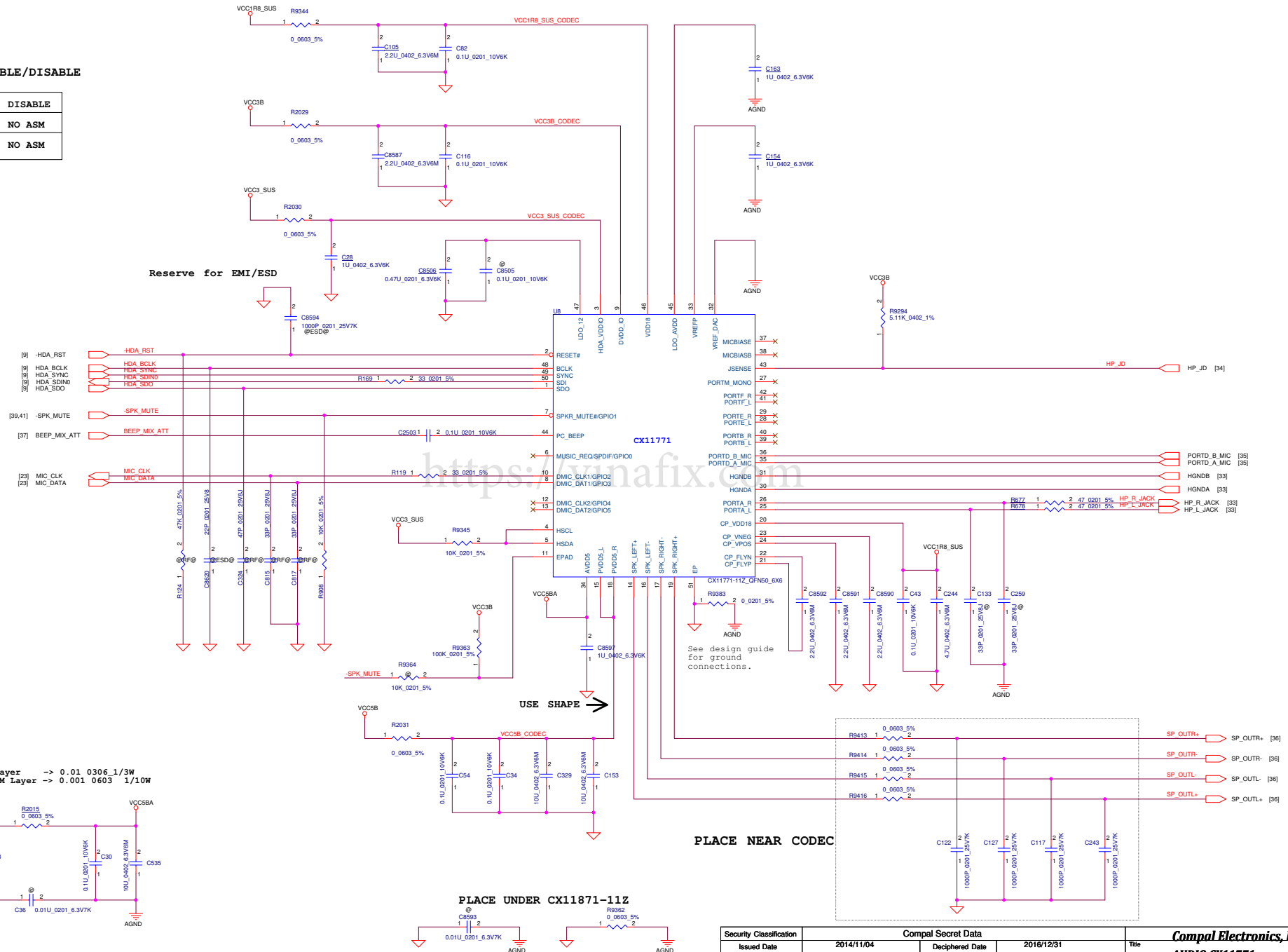
<https://vinafix.com>

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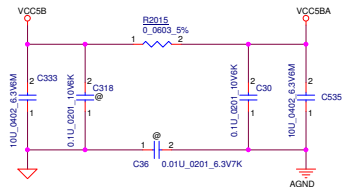
TABLE MIC HW ENABLE/DISABLE

| | ENABLE | DISABLE |
|------|--------|---------|
| R961 | ASM | NO ASM |
| R119 | ASM | NO ASM |

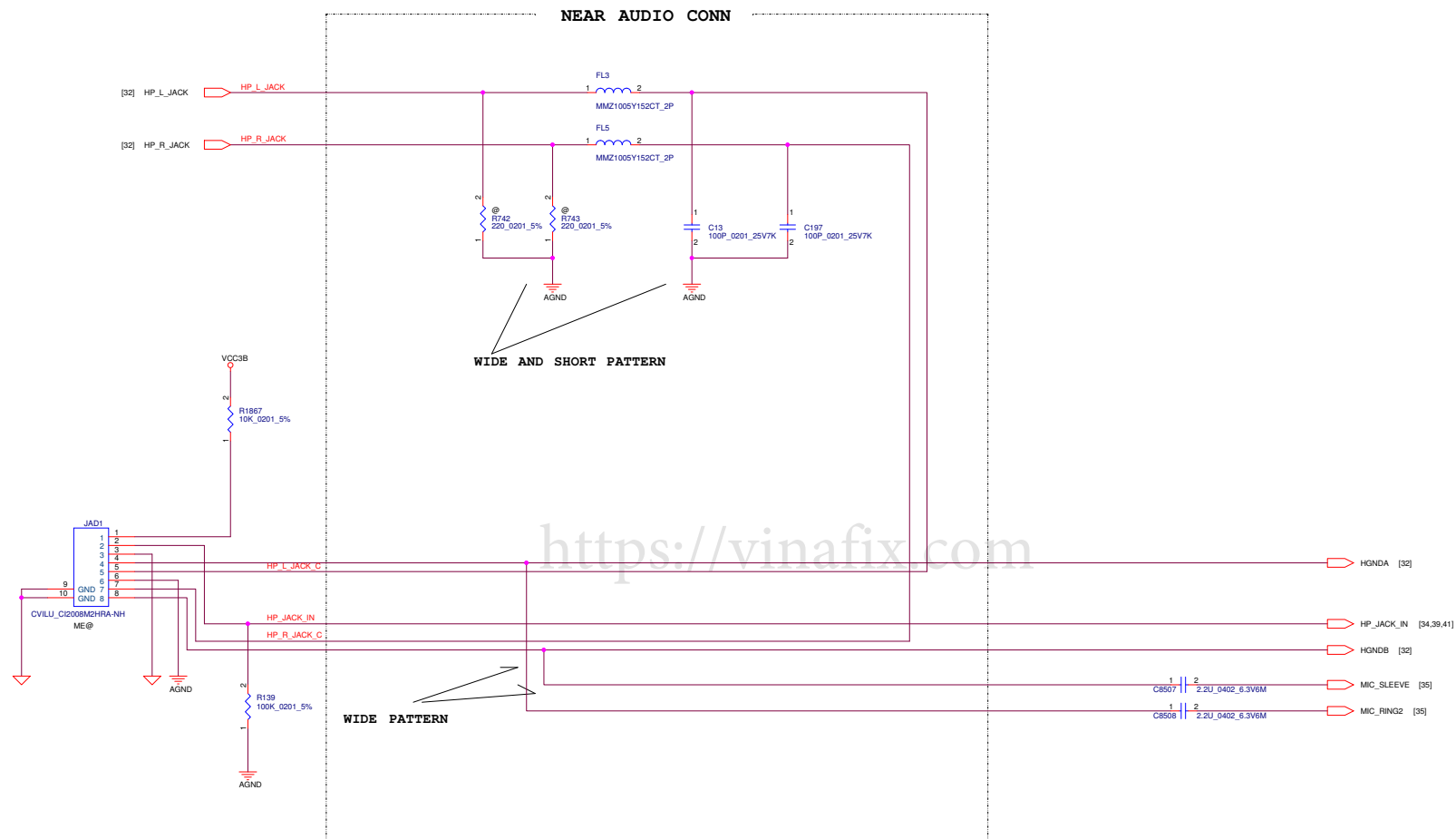
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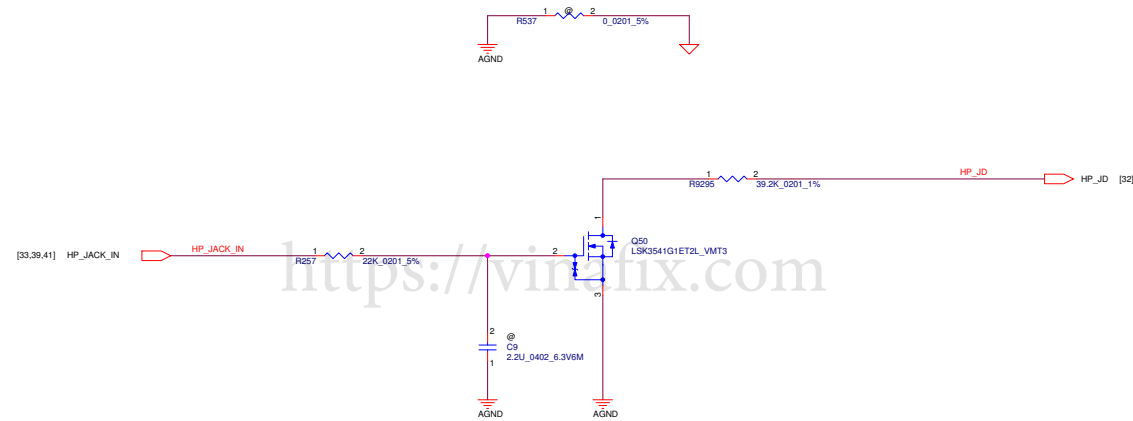
R2015
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Place BOTTOM Layer -> 0.001 0603 1/10W



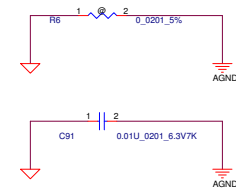
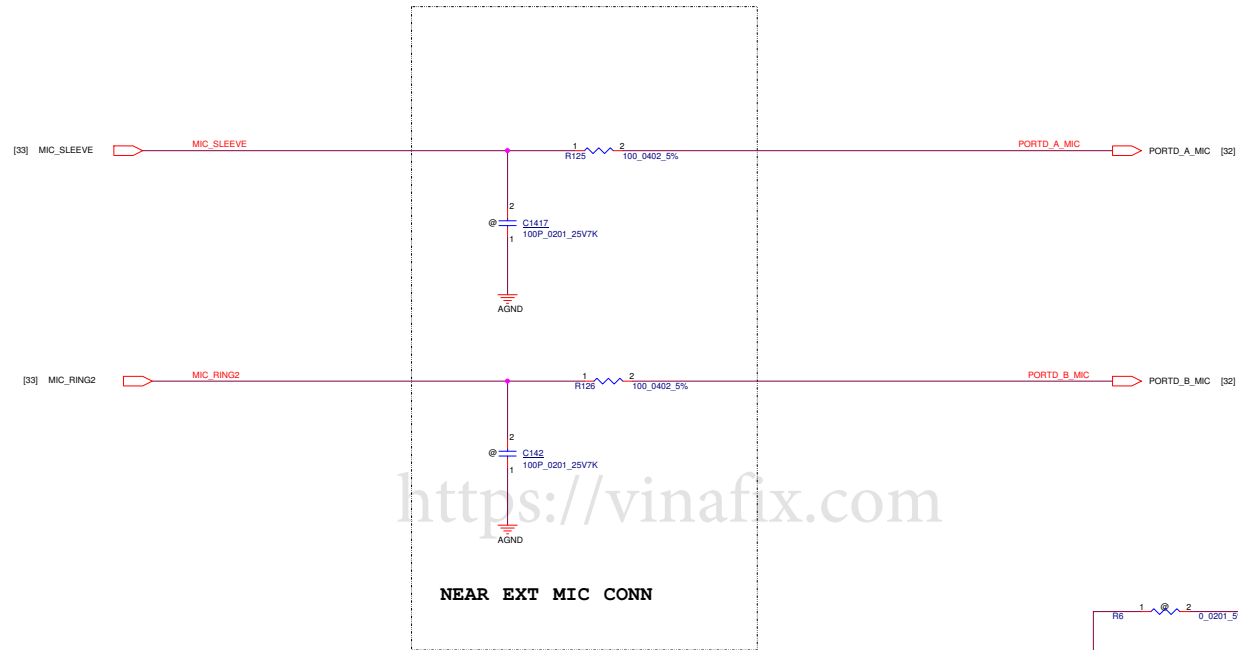
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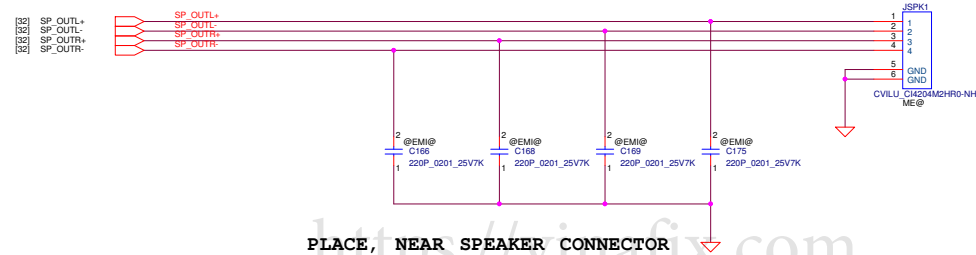
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| Date: Tuesday, May 03, 2016 | | | | Rev 0.5 |
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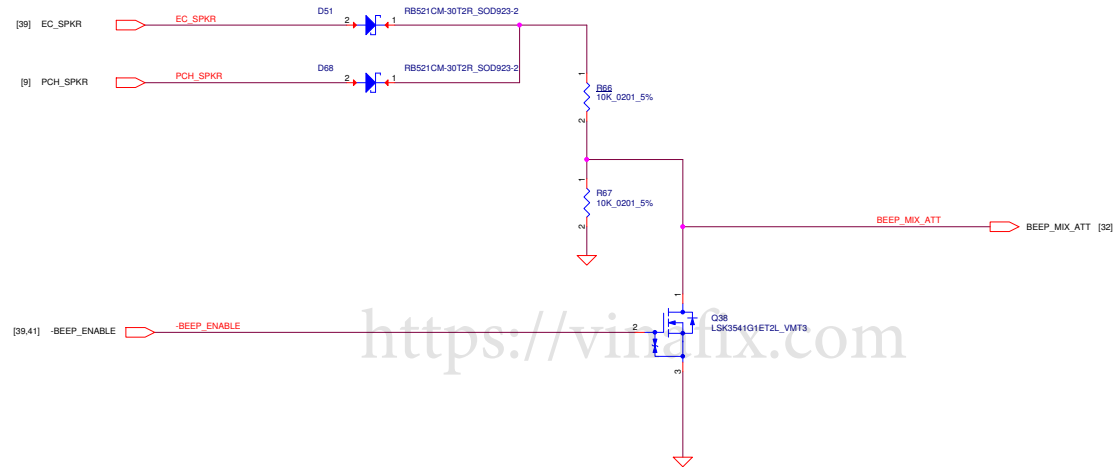
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| | | | | Date: Tuesday, May 03, 2016 | Sheet 34 of 75 |



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| | | | | Date | Tuesday, May 03, 2016 |
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| Size | | Document Number | | Rev | |
| Custom | | LA-EZ92P | | 0.1 | |
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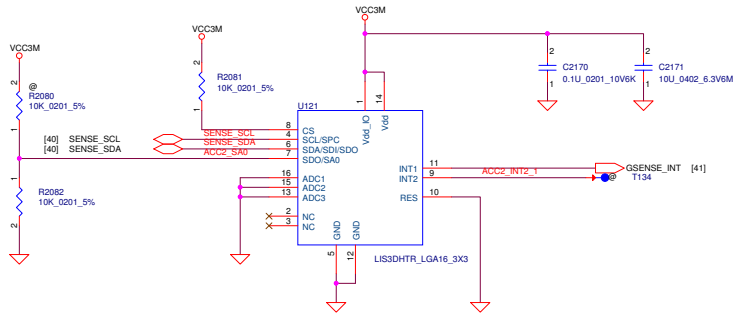
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| | | | | Document Number | 0.1 |
| | | | | Custom | LA-E292P |
| | | | | Date | Tuesday, May 03, 2016 |
| | | | | Sheet | 37 of 75 |

TABLE

| ACC2_SA0 | Address Selection |
|----------|-------------------|
| H | 32h (W) & 33h (R) |
| L | 30h (W) & 31h (R) |

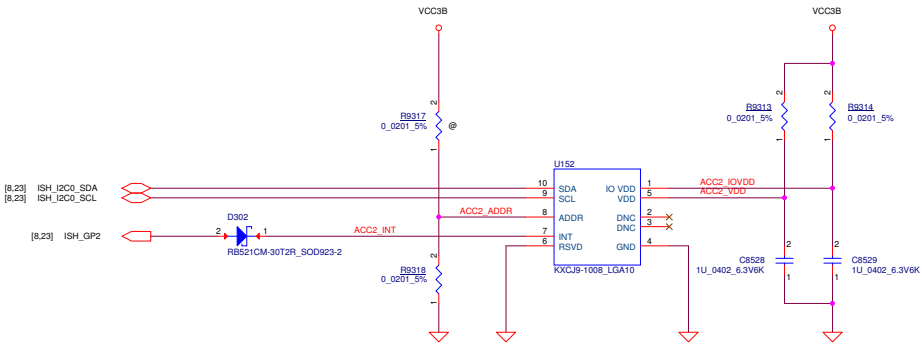
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| CS | Mode Selection |
|----|----------------|
| H | I2C Mode |
| L | SPI Mode |



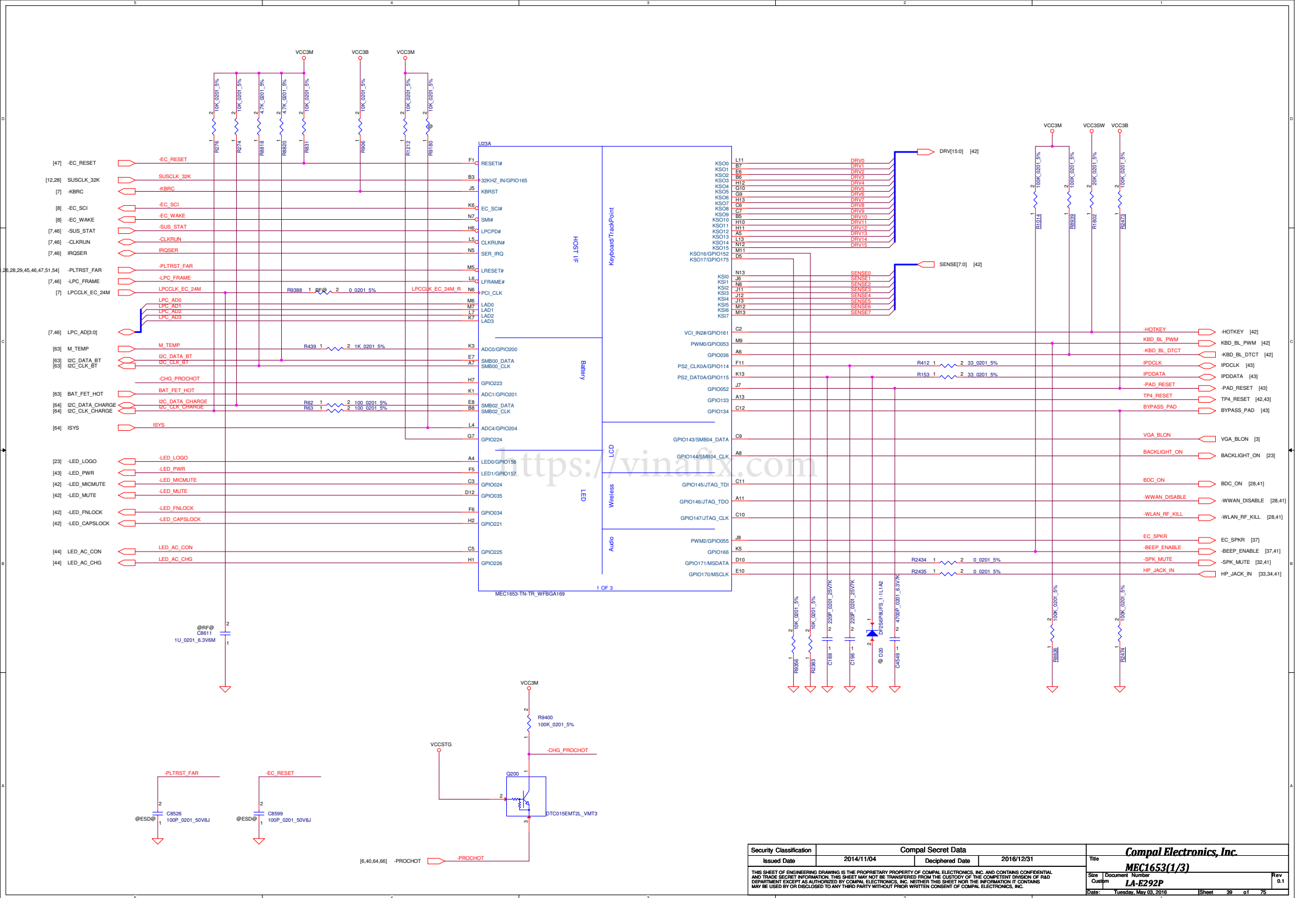
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<https://vinafix.com>

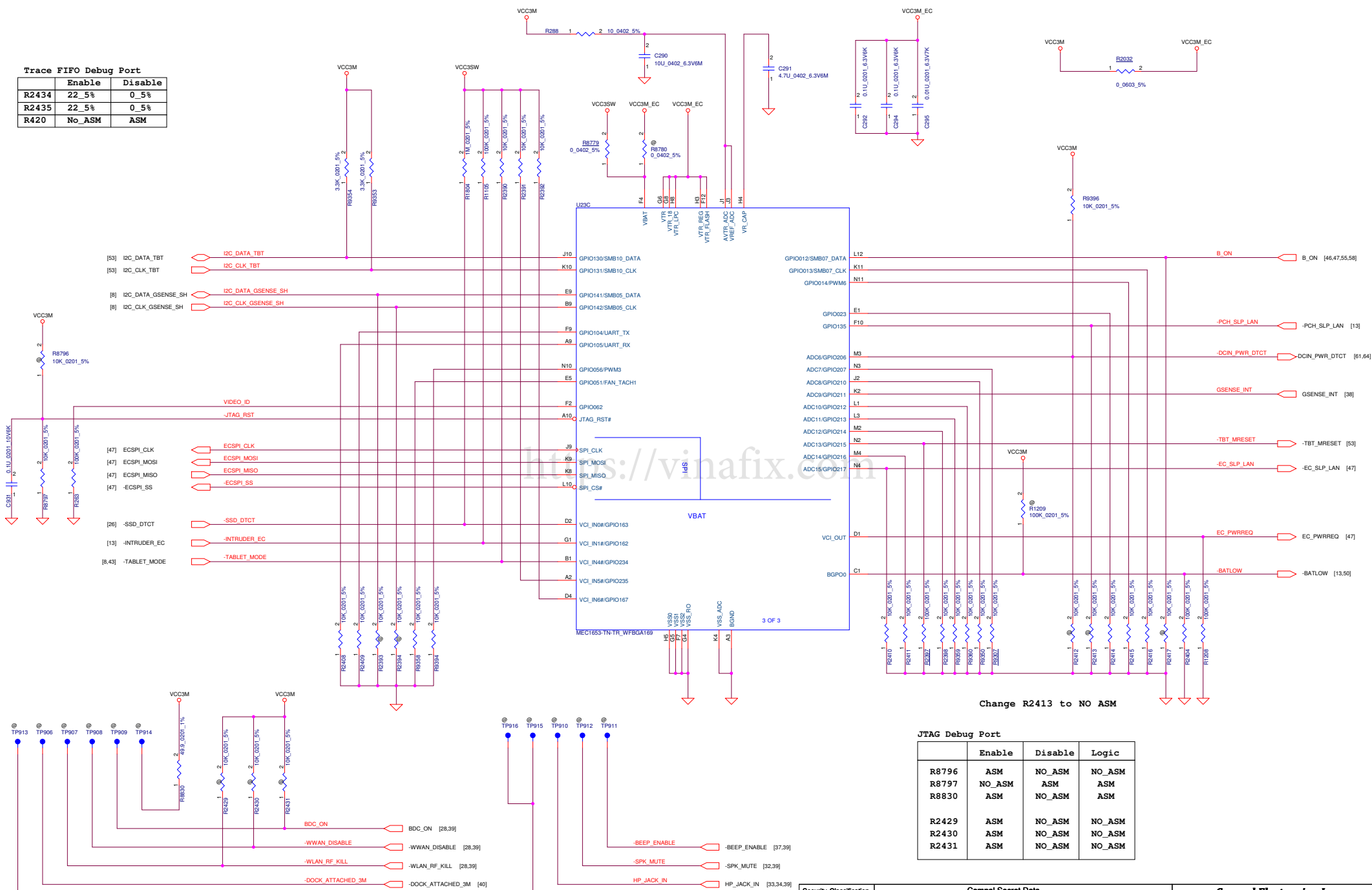


KXCJ9 Address: 0x1Ch

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| Date: Tuesday, May 03, 2016 | | | | Rev 0.1 |
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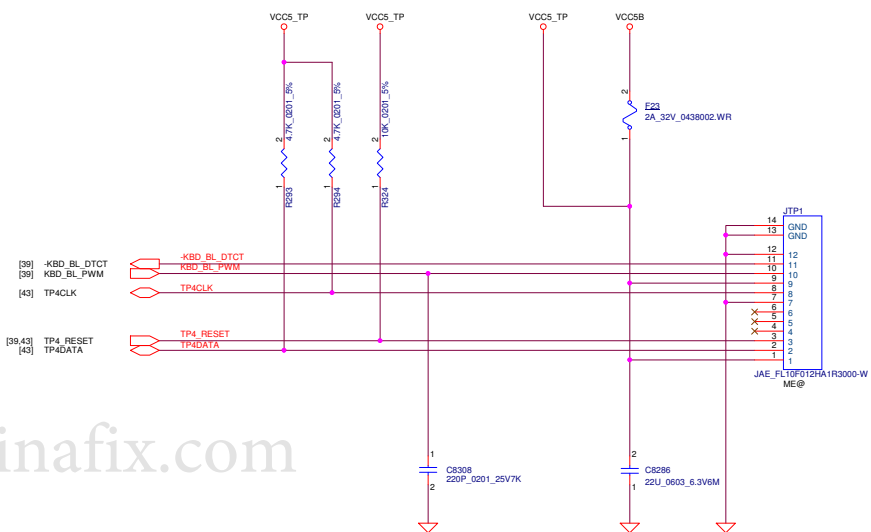


| Trace FIFO Debug Port | | |
|-----------------------|--------|---------|
| | Enable | Disable |
| R2434 | 22_5% | 0_5% |
| R2435 | 22_5% | 0_5% |
| R420 | No_ASM | ASM |



| JTAG Debug Port | | | |
|-----------------|--------|---------|--------|
| | Enable | Disable | Logic |
| R8796 | ASM | NO_ASM | NO_ASM |
| R8797 | NO_ASM | ASM | ASM |
| R8830 | ASM | NO_ASM | ASM |
| R2429 | ASM | NO_ASM | NO_ASM |
| R2430 | ASM | NO_ASM | NO_ASM |
| R2431 | ASM | NO_ASM | NO_ASM |

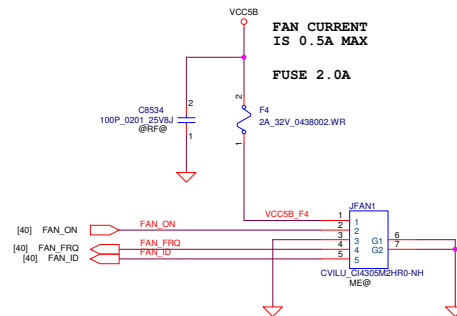
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| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | |
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| | | | Size Custom | Rev 0.1 |
| | | | Date | 12/29/2016 |
| | | | Sheet | 41 of 75 |



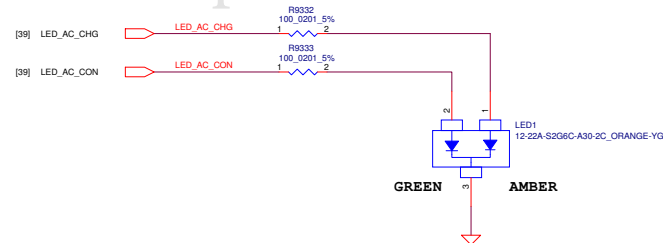
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| | | | | Custm | LA-F292P | 0.1 |
| | | | | Date: | Tuesday, May 03, 2016 | Sheet 42 of 75 |



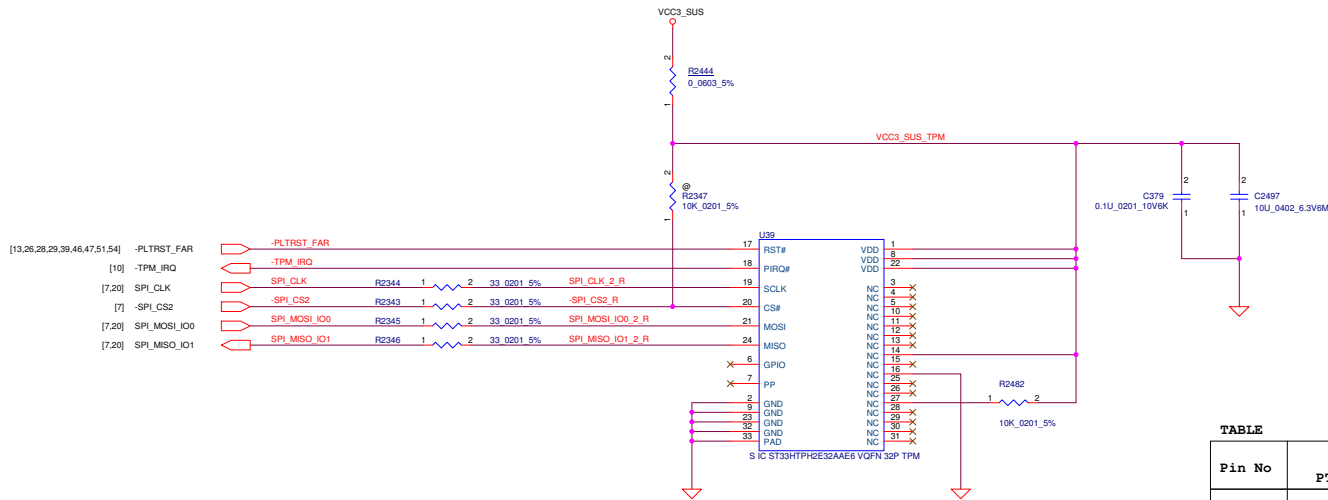
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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. TOUCH PAD/NFC/BUTTON/PEN I | | Title | |
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| | | | | L4-E292P | | | |
| Date: Tuesday, May 29, 2014 | | | | Sheet: 43 of 75 | | | |



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| | | | | Custom | 0.1 |
| | | | | Date | Tuesday, May 03, 2016 |
| | | | | Sheet | 44 of 75 |



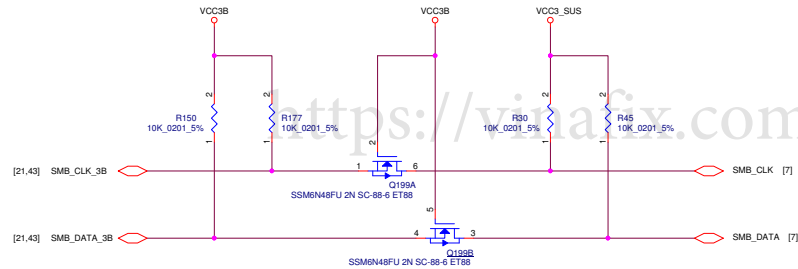
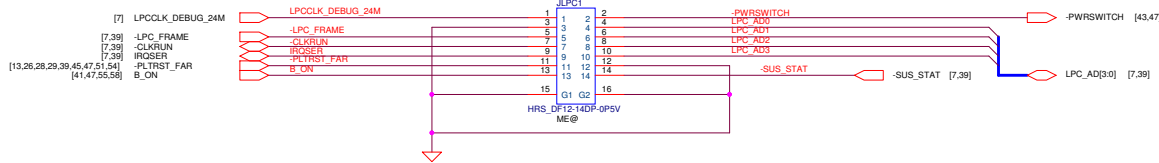
-Change TPM1.2 to TPM2.0
-Infineon SLB9670VQ2.0 part number SA00009N200
-ST ST33HTPH2E32AAE6 part number SA00009S000

TABLE

| Pin No | TCG PTP Spec (v38) | Infineon SLB9670VQ1.2 FW 6.40 | Nuvoton NPCT650LB0YX |
|--------|-----------------------|----------------------------------|-------------------------|
| 1 | VDD | VDD | VSB |
| 2 | GND | GND | NC |
| 3 | GPIO | NC | GPX/GPIO2 |
| 4 | GPIO | NC | PP |
| 5 | NC | NC | TEST |
| 6 | VNC/GPIO | GPIO | GPI03 |
| 7 | GPIO/VDD | PP | NC |
| 8 | VDD | VDD | VDD |
| 9 | GND | GND | GND |
| 10 | VNC | NC | NC |
| 11 | NC | NC | NC |
| 12 | NC | NC | Reserved |
| 13 | VNC/GPIO | NC | GPI04 |
| 14 | VDD | NC | VDD |
| 15 | NC | NC | DNC |
| 16 | GND | NC | GND |
| 17 | SPI_RST# | RST# | SPI_RST# |
| 18 | SPI_PIRQ# | PIRQ# | SPI_PIRQ# |
| 19 | SPI_CLK | SCLK | SCLK |
| 20 | SPI_CS# | CS# | SCS# |
| 21 | MOSI | MOSI | MOSI |
| 22 | VDD | VDD | VDD |
| 23 | GND | GND | GND |
| 24 | MISO | MISO | MISO |
| 25 | NC | NC | NC |
| 26 | NC | NC | NC |
| 27 | NC | NC | (SERIRQ) |
| 28 | NC | NC | DNC |
| 29 | VNC/ GPIO | NC | GPI00 |
| 30 | VNC/ GPIO | NC | GPI01 |
| 31 | VNC | NC | NC |
| 32 | GND | GND | GND |

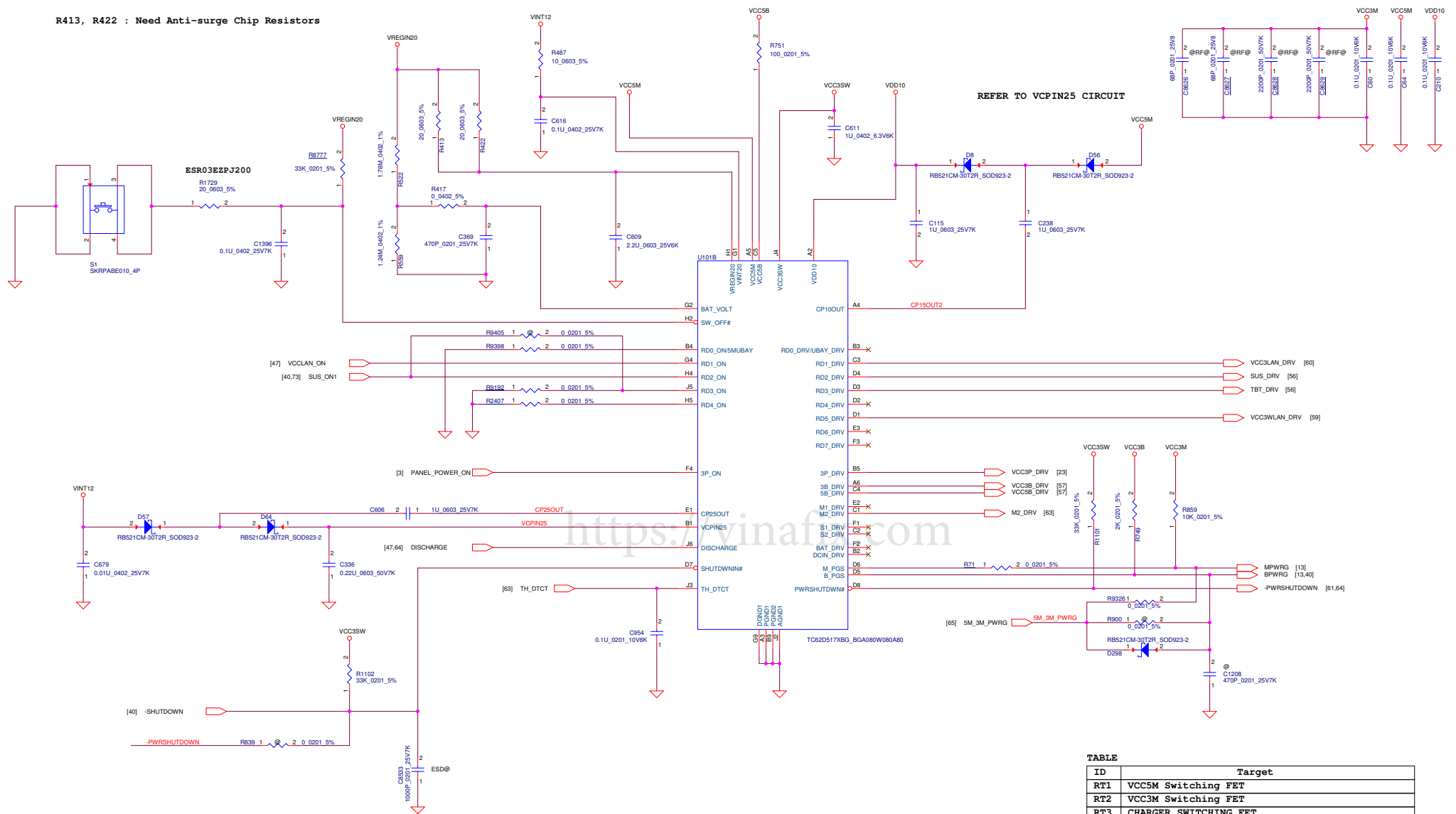
| TABLE | | | |
|-------|-----|--------|---------|
| REF | DES | ENABLE | DISABLE |
| JLPC1 | | ASM | NO_ASM |
| R220 | | ASM | NO_ASM |

↑
LOGIC



| | | | | | |
|---|------------|--------------------|------------|--------------------------|-----------------------|
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| | | | | Custom | LA-E292P |
| | | | | Date | Tuesday, May 03, 2016 |
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R413, R422 : Need Anti-surge Chip Resistors



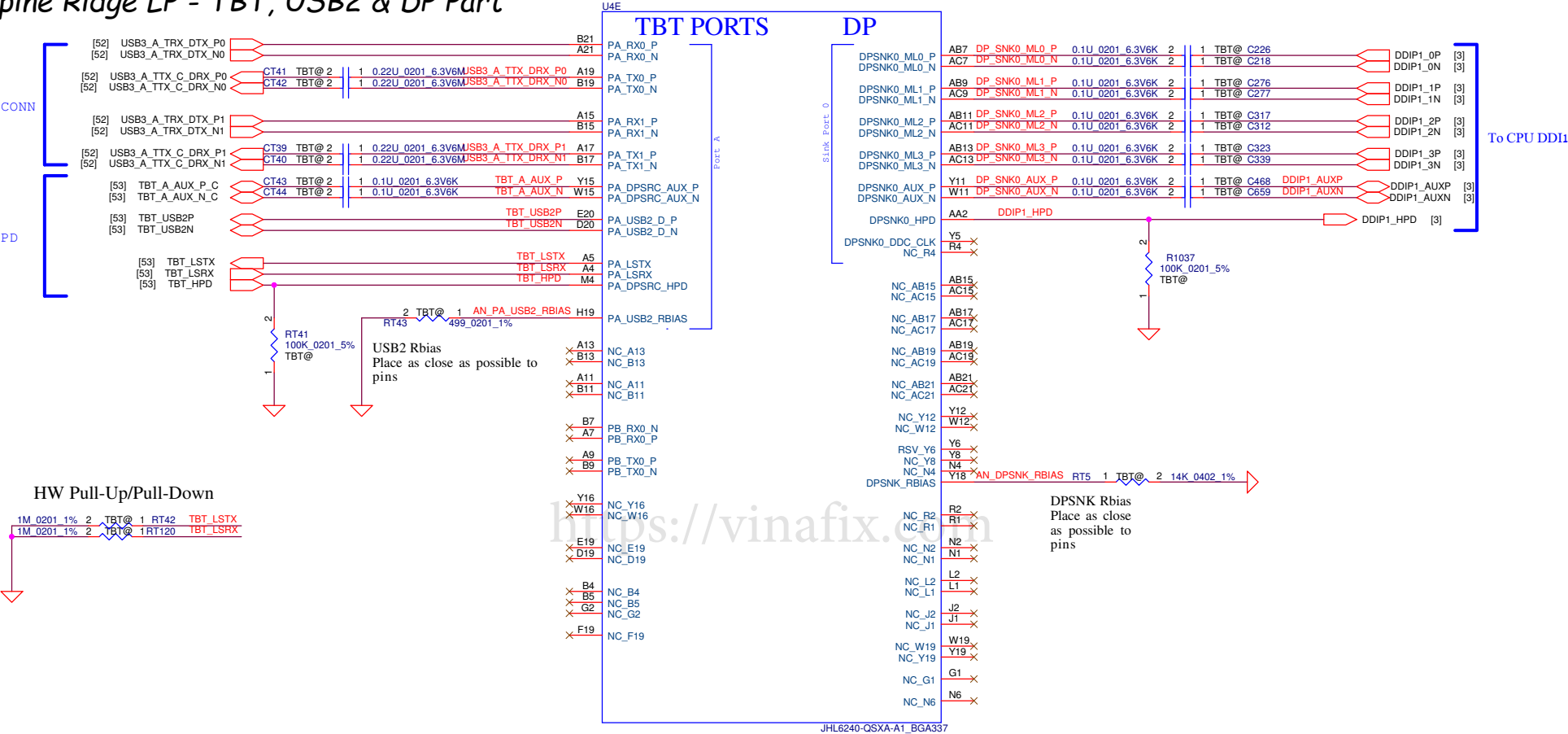
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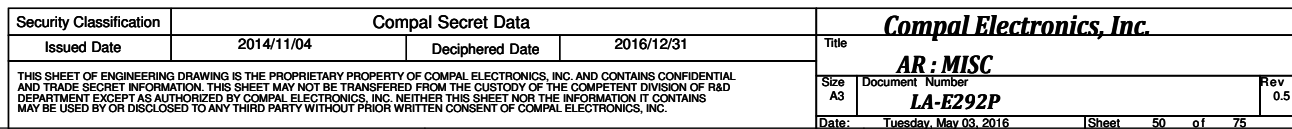
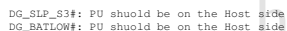
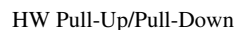
| ID | Target |
|------|--------------------------------------|
| RT1 | VCC5M Switching FET |
| RT2 | VCC3M Switching FET |
| RT3 | CHARGER SWITCHING FET |
| RT4 | M_BAT_PWR to BAT_PWR12 FET |
| RT5 | CHAGEROUT12 to BAT_PWR12 FET |
| RT6 | VCCSA MOSFET Driver NCP81382 |
| RT7 | VCCCPUCORE MOSFET Driver NCP81382 |
| RT8 | VCCCGFXCORE-I MOSFET Driver NCP81382 |
| RT9 | CPU Die |
| RT10 | DOCK_PWR20 IN to DOCK_PWR20 FET |
| RT11 | DCIN_PWR20 F to CV20_FET |

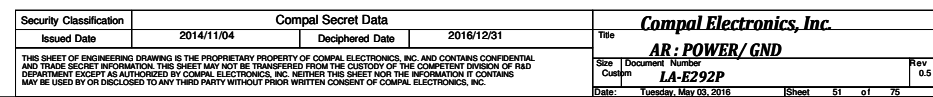
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| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | Compel Electronics, Inc. THINK ENGINE(2/2) | |
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| | | | | Custodian | 0.1 |
| | | | | Date | |
| | | | | Issued | |
| | | | | 48 | 75 |

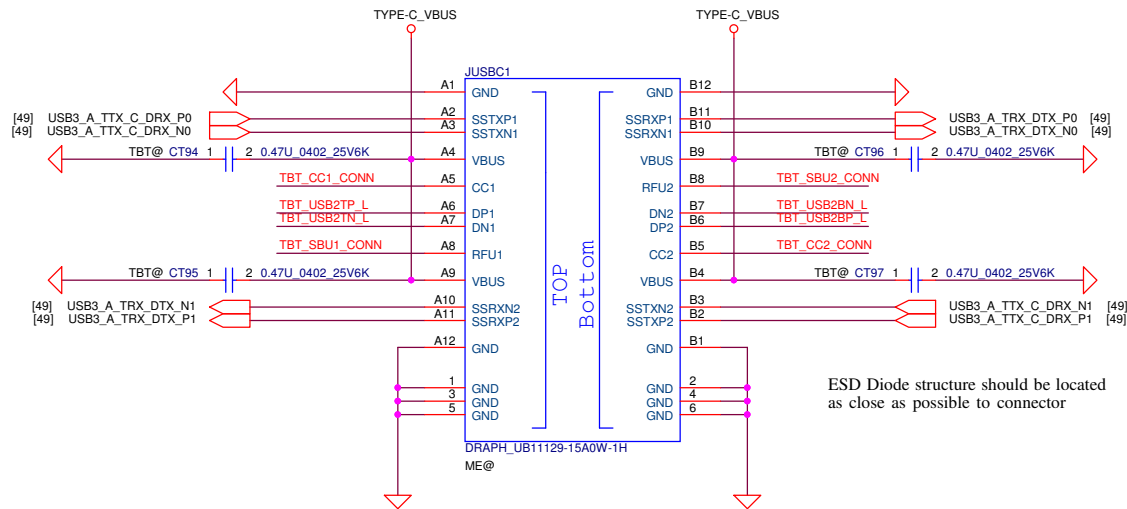
Alpine Ridge LP - TBT, USB2 & DP Part

Alpine Ridge LP - TBT, USB2 & DP Part



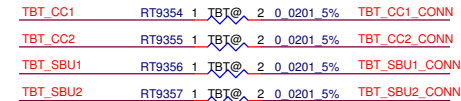
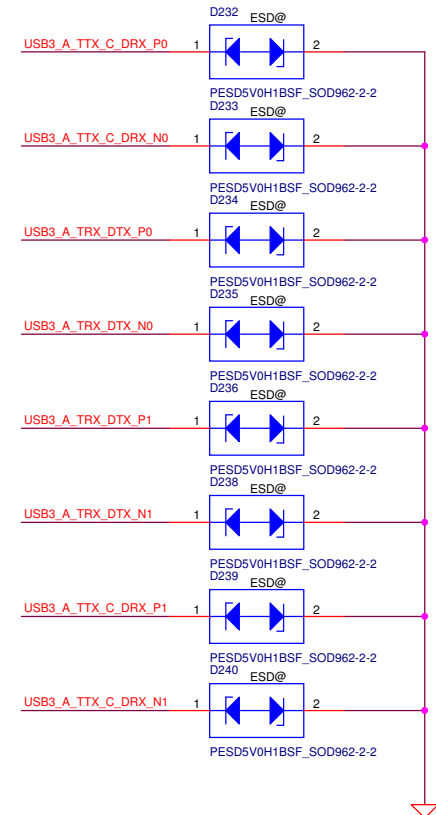
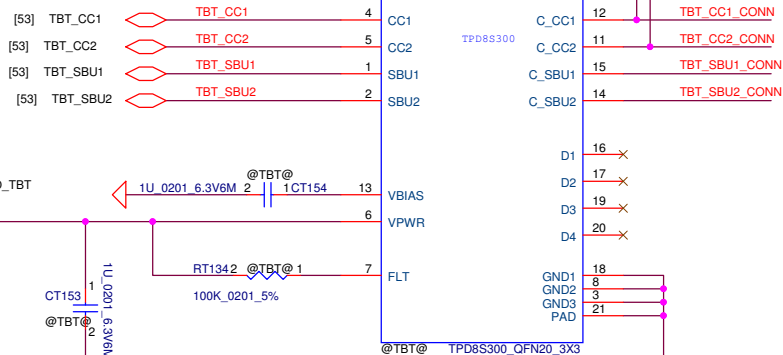
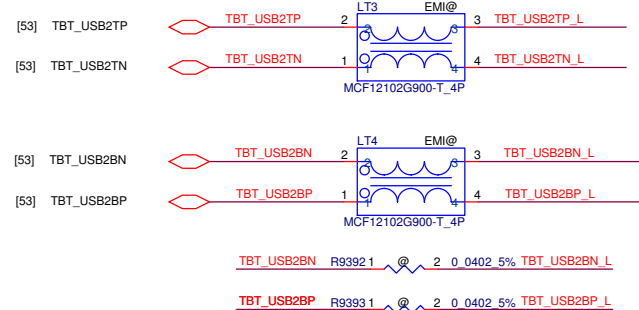
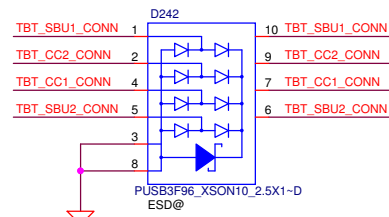
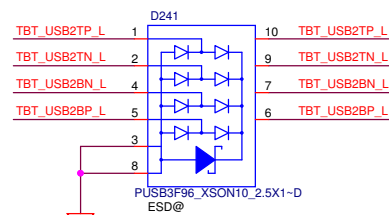
Alpine Ridge LP - Misc
Symbol

Alpine Ridge SP - VCC
SymbolAlpine Ridge LP - PCIe
Symbol

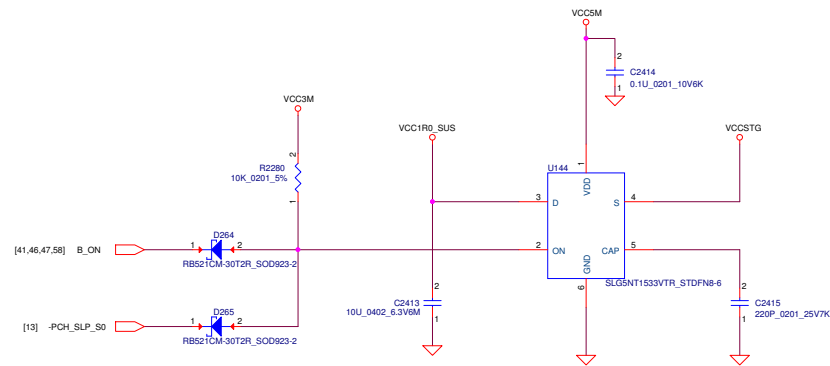
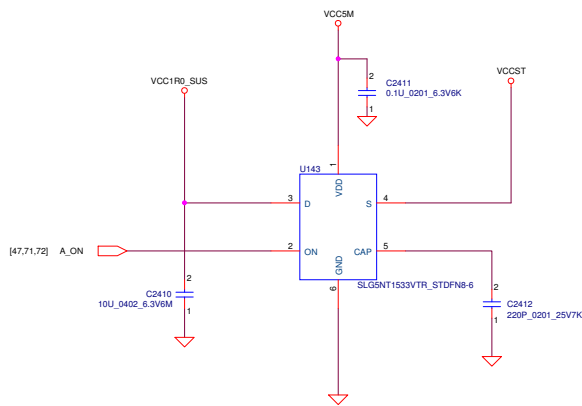


ESD Diode structure should be located as close as possible to connector

ESD for USB2 Lines and Control lines

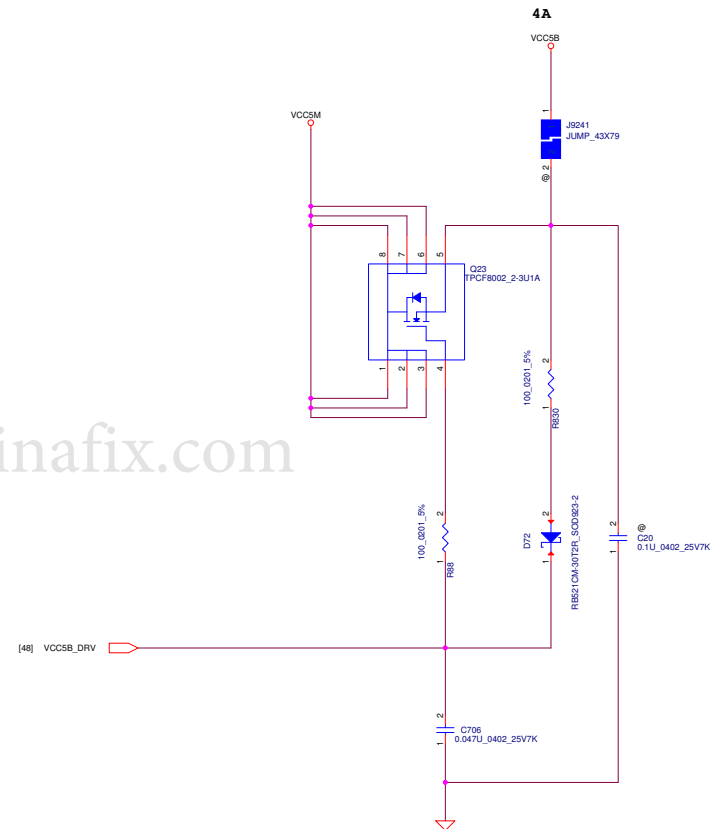
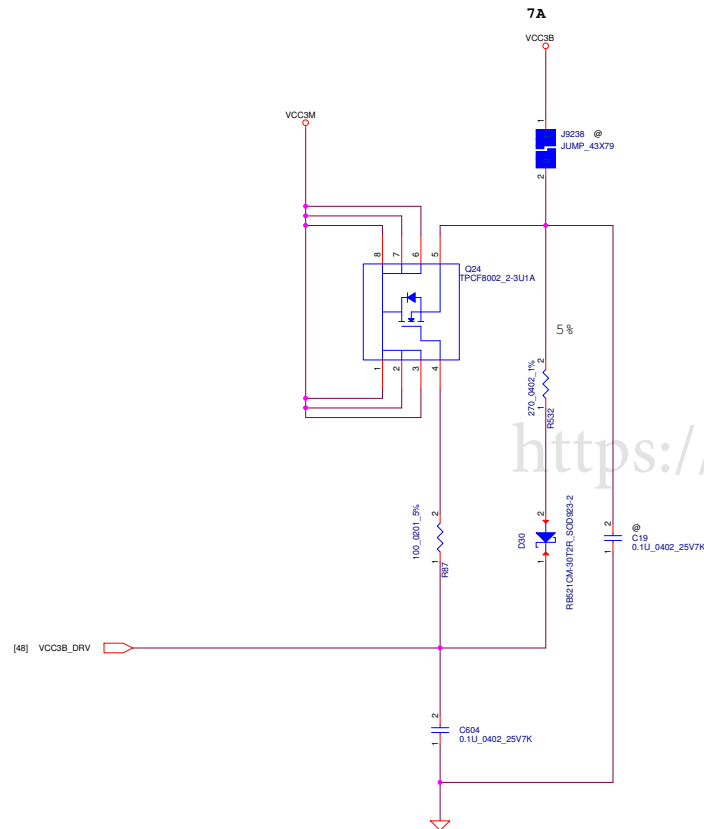


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| Size A3 | Document Number | LA-E292P | | Rev 0.5 | |
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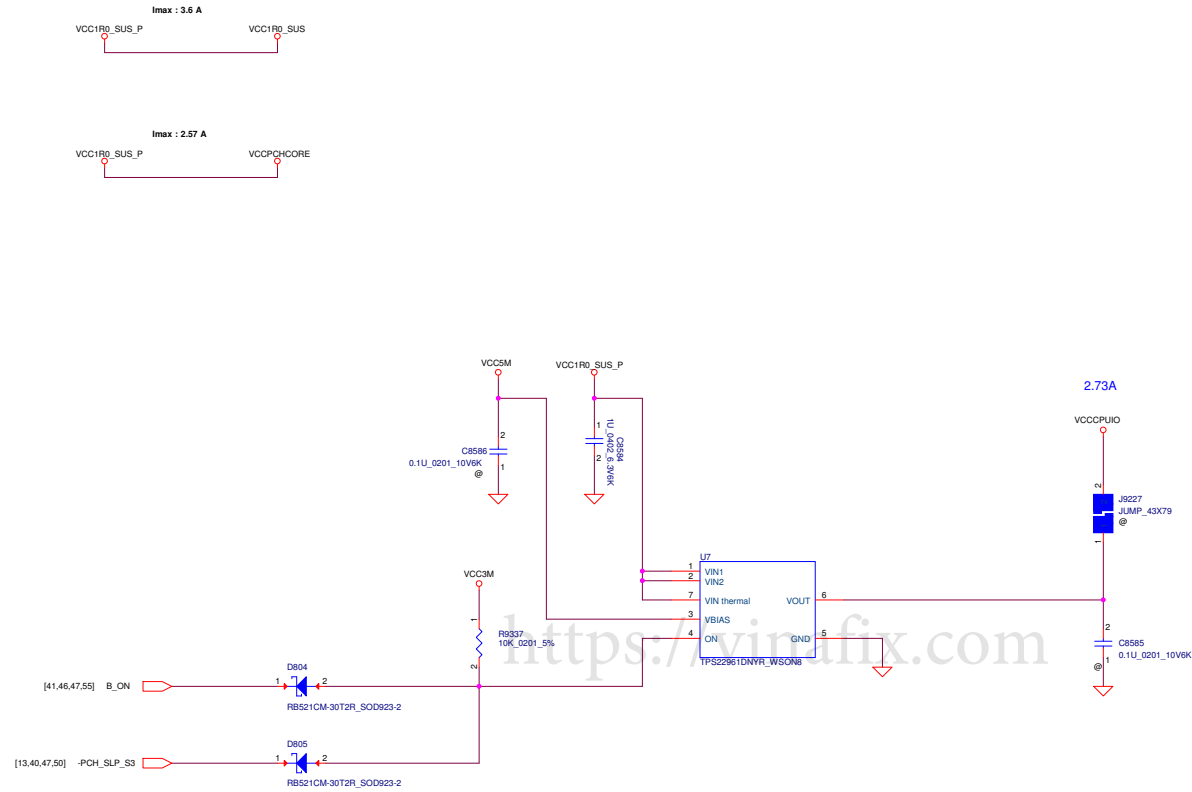


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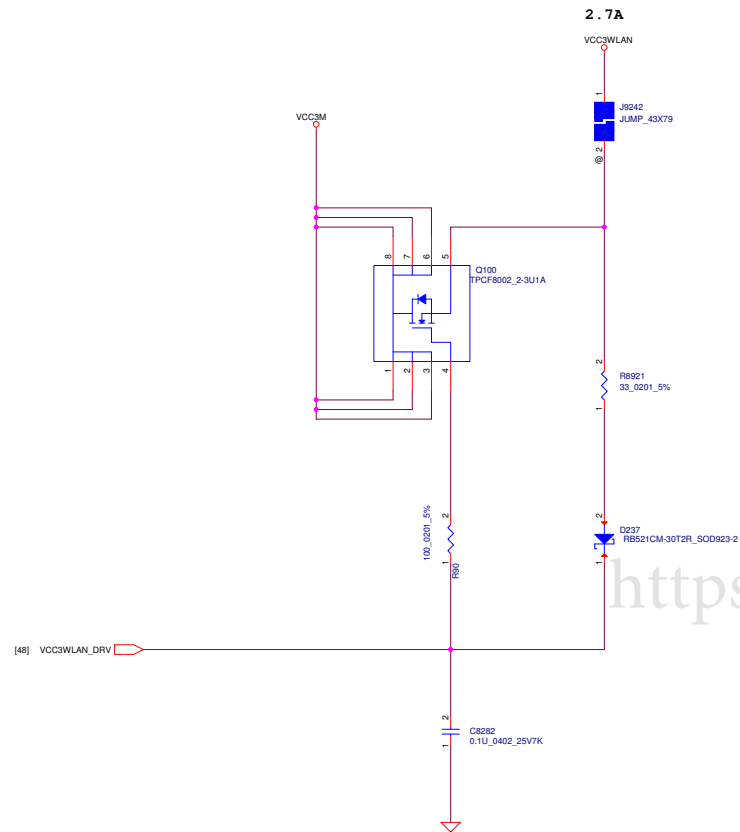
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| | | | | Custom | LA-E292P |
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|---|--------------------|-----------------|------------|--------------------------|------------|
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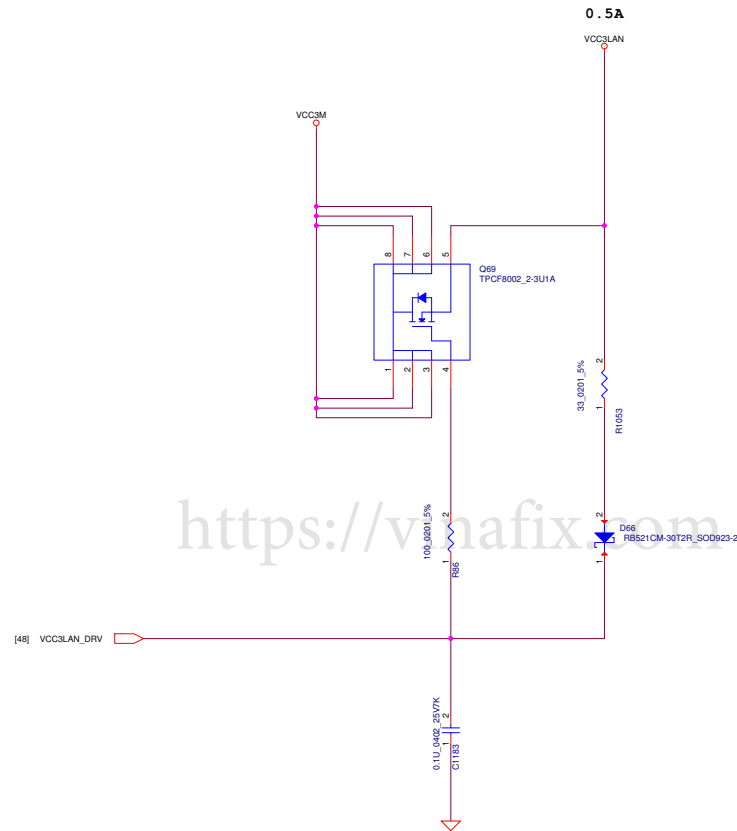


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| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | Title | LOAD SW VCCCPU10 |
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| | | | | Custom | 0.1 |
| | | | | Date | Tuesday, May 03, 2016 |
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| | | | | Document Number | 0.5 |
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| | | | | Date | Tuesday, May 03, 2016 |
| | | | | Sheet | 59 of 75 |



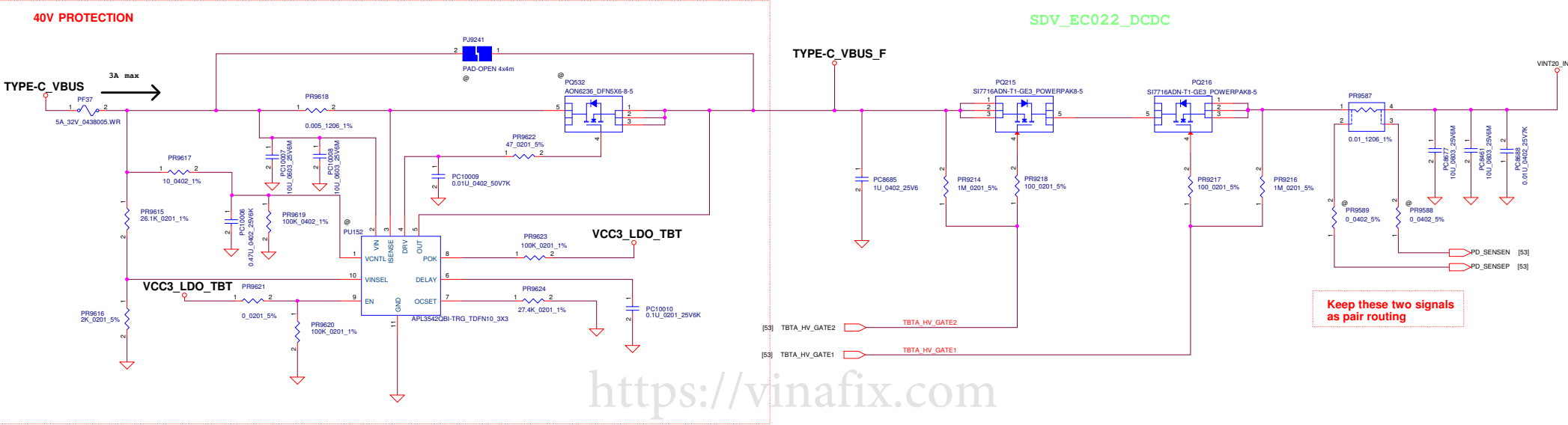
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| | | Custom LA-E292P | | 0.5 | |
| Date | | Tuesday, May 03, 2016 | | Sheet 69 of 75 | |

SDV_EC023_DCDC



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|--|--|--------------------|--|-----------------|--|------------|--|------|--|---------------------------------|--|-----------------------|--|-------|--|----------|--|
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| Issued Date | | 2014/11/04 | | Deciphered Date | | 2016/12/31 | | Size | | | | Rev | | | | | |
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| | | | | | | | | | | Document Number | | LA-E292P | | | | | |
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SDV_EC026_DCDC
SDV_EC028_DCDC



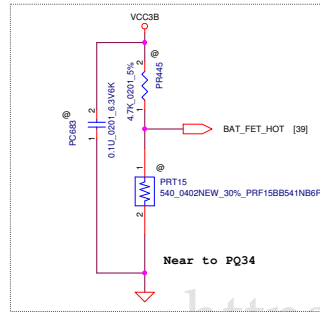
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| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | Title | TYPE-C IN |
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| Custom | | | Tuesday, May 03, 2018 | | Sheet 62 of 75 |

MAIN BAT CONN

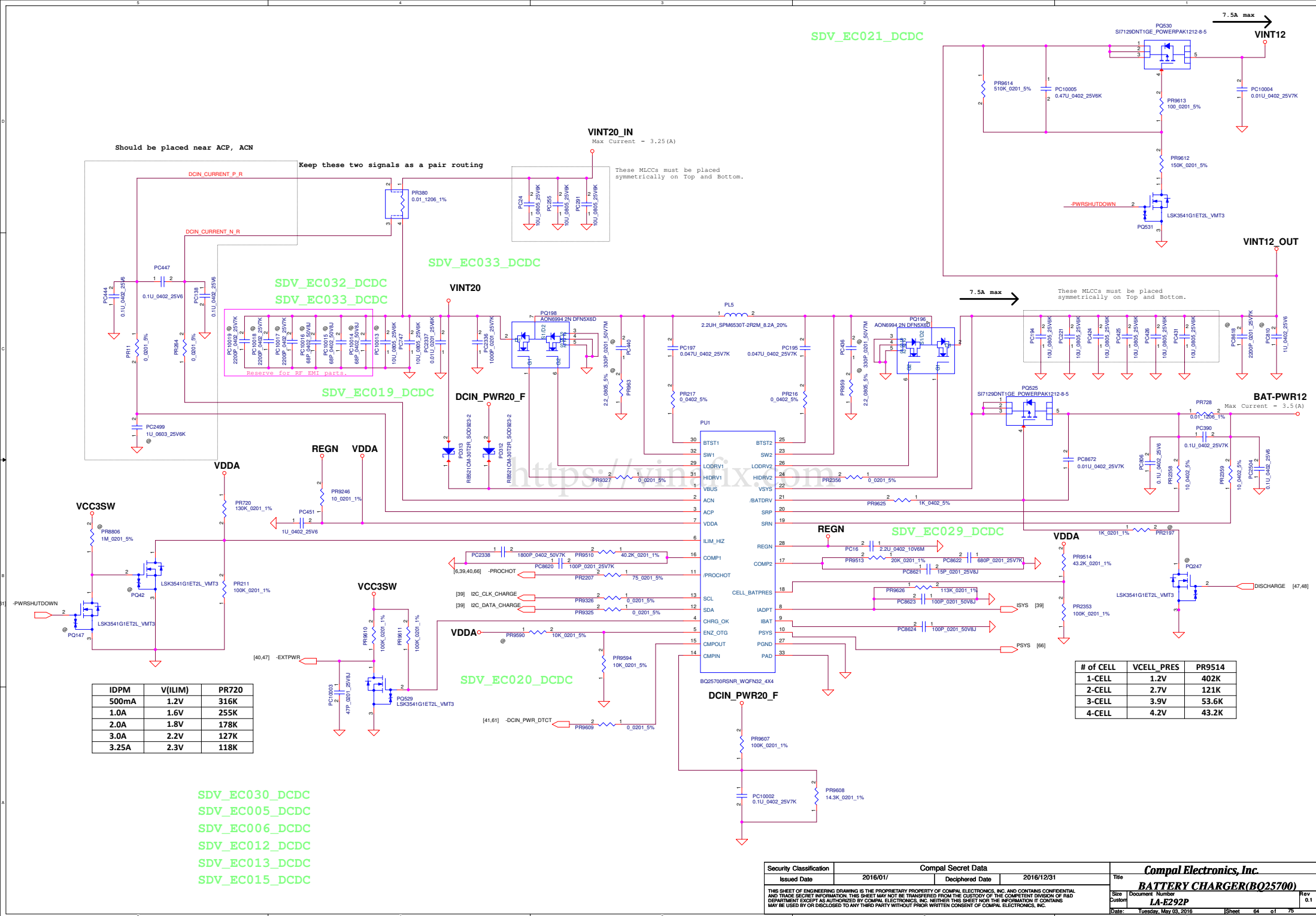
The diagram illustrates the main battery connection for the M2M module. It shows the connection of the battery to the module's power pins (M BAT IN, M-BAT-PWR, M-TEMP) and the internal power management components.

Key Components and Connections:

- Battery Connector (PJBATT):** A 12-pin connector with pins 1-9 connected to the module's power pins. Pin 10 is GND and Pin 11 is GND.
- Power Input (M BAT IN):** Connected to the battery's positive terminal (pin 1 of PJBATT).
- Power Regulation:** The input is connected to a series of capacitors (390F_0.01_50V7K, 2200F_0.01_50V7K, 390F_0.01_50V7K, 2200F_0.01_50V7K) and a diode (PC207) to regulate the voltage.
- Temperature Sensor (M_TEMP):** Connected to the module's temperature pin (pin 39 of the M2M module).
- Power Management ICs:** The diagram shows the internal power management ICs, including the M2M module (M2M) and the M2M module (M2M).
- Output (M-BAT-PWR):** The regulated power is output to the M-BAT-PWR pin (pin 39 of the M2M module).
- Other Components:** The diagram also shows other components like the M2M module (M2M) and the M2M module (M2M).

[illegible][illegible][illegible]

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|---|--------------------|-----------------|------------|--------|-----------------------|---------------------------------|----------|
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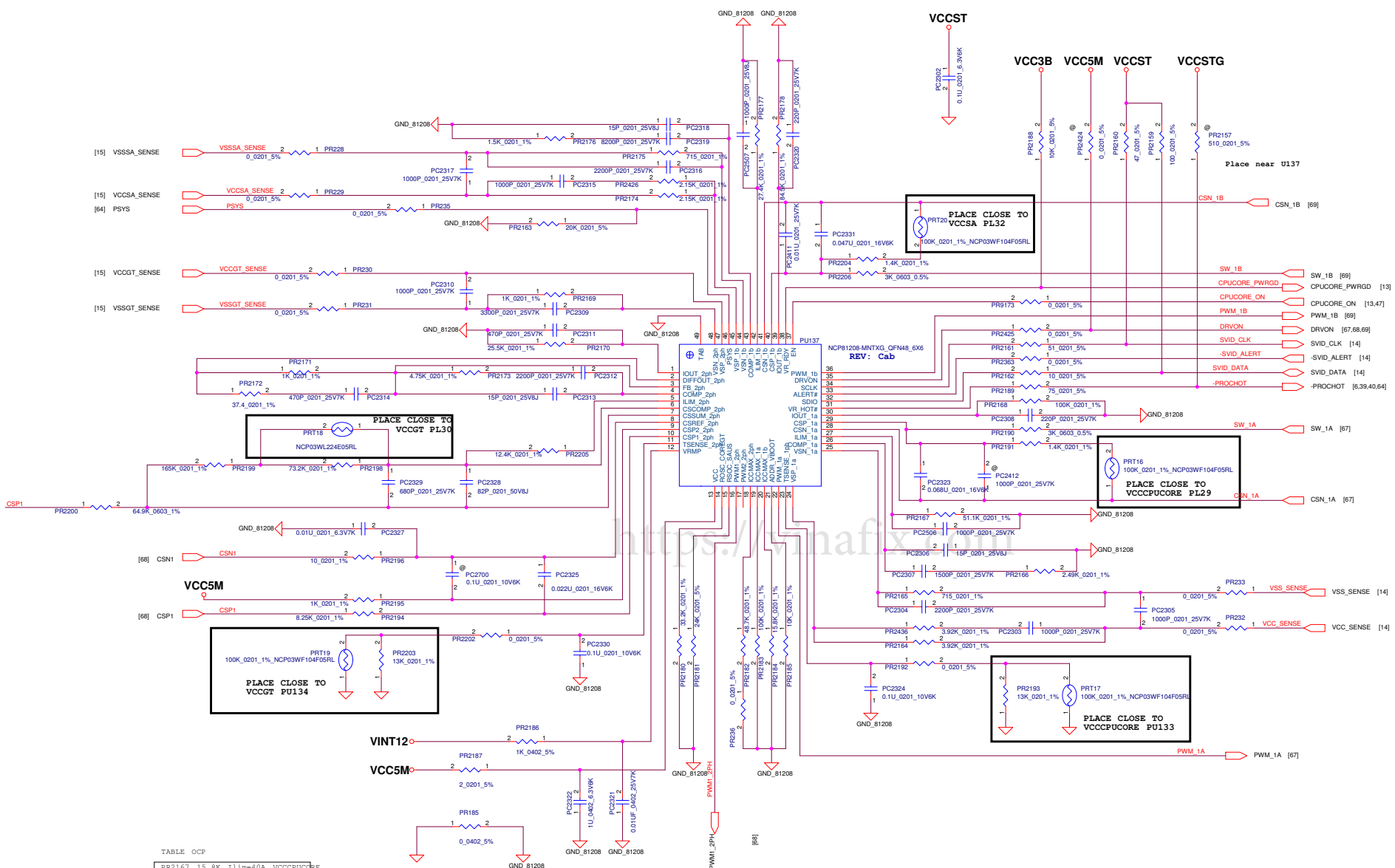
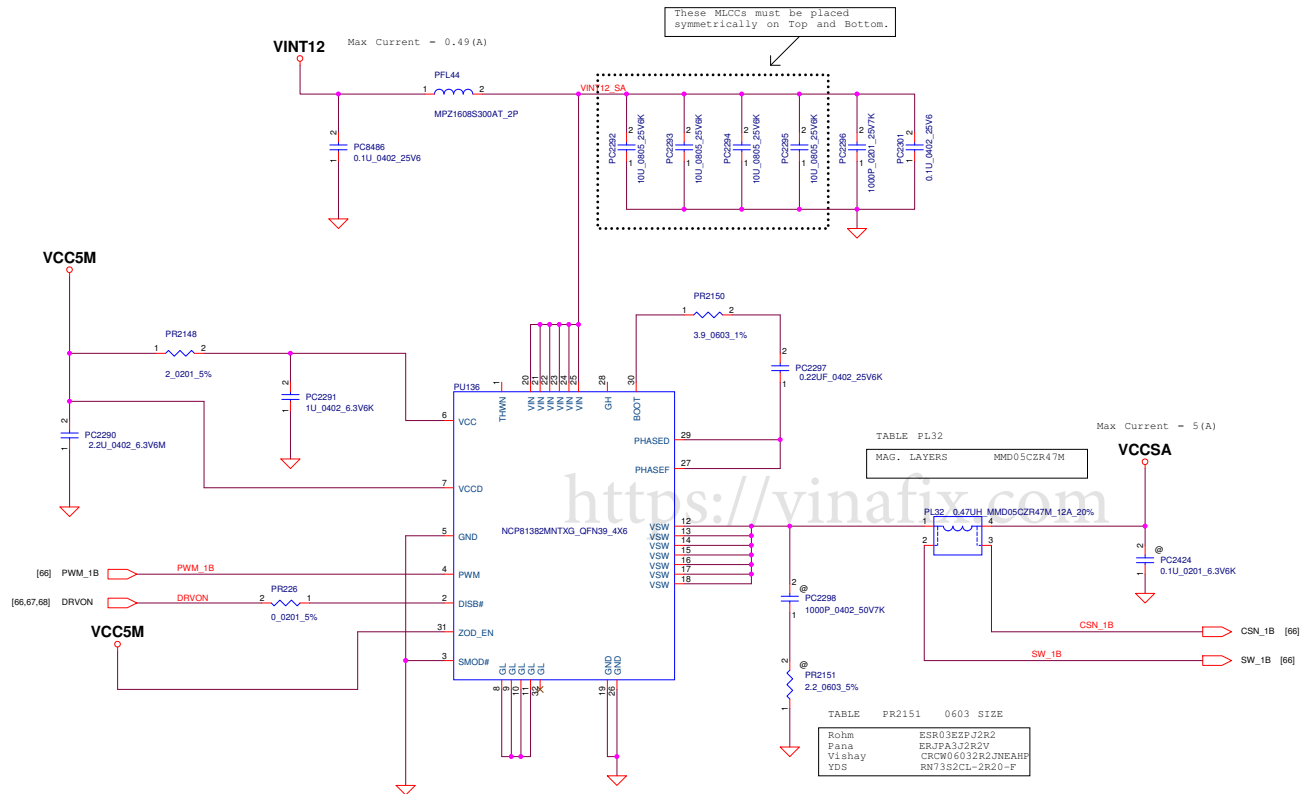
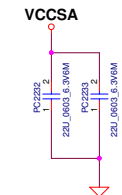
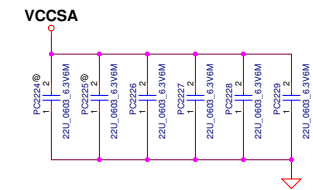


TABLE OCP

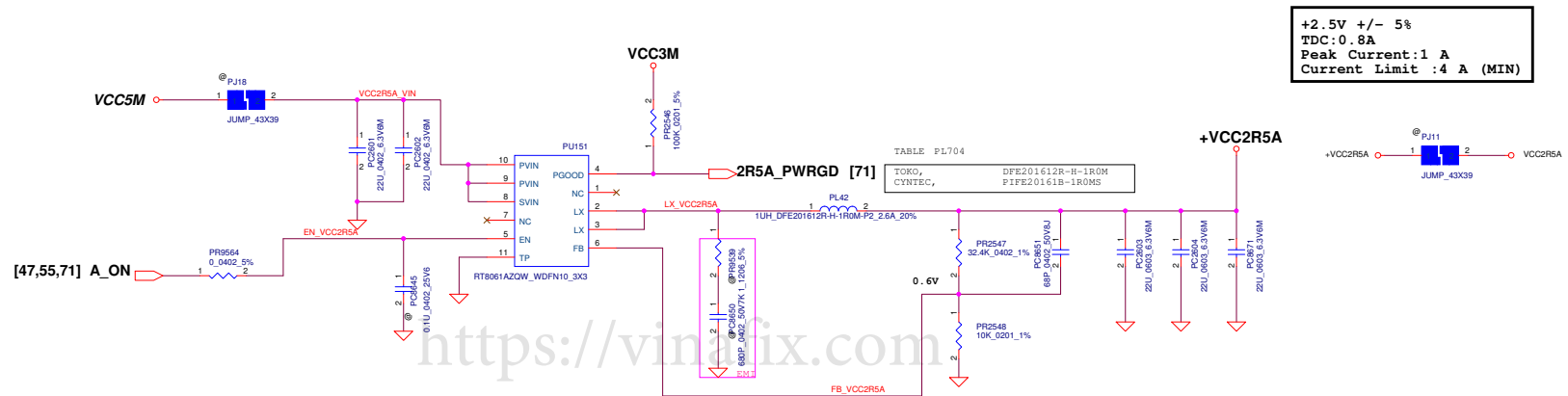
| | | | |
|--------|-------|----------|------------|
| PR2167 | 15.8K | Ilim=40A | VCCFCUCORE |
| PR2205 | 12.4K | Ilim=40A | VCCFCUCORE |
| PR2177 | 27.4K | Ilim=10A | VCCSA |



6pcs (+2pcs) 22uF for VCCSA

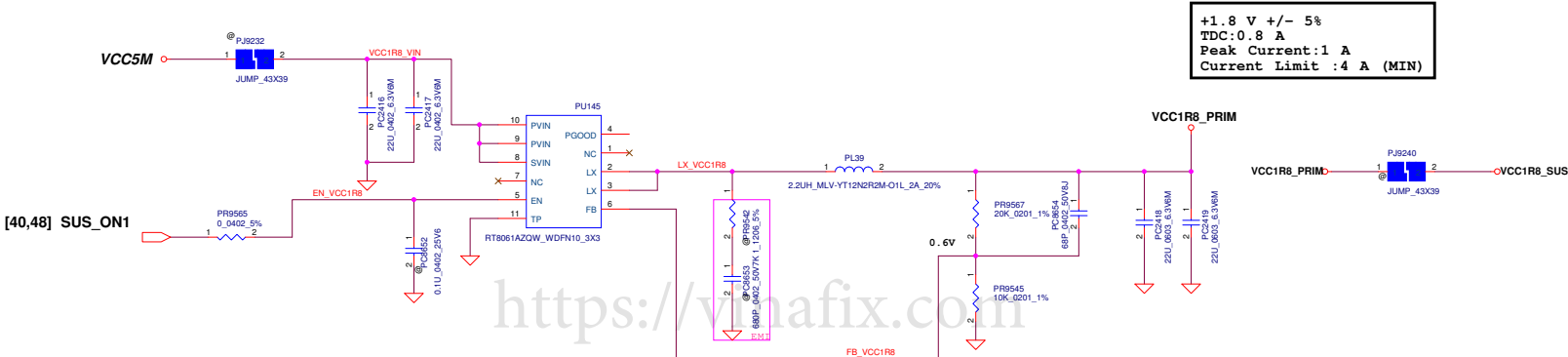


SDV_EC010_DCDC



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|--|--------------------|-----------------|------------|-----------------------|--------------------------|----------------|
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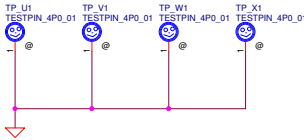
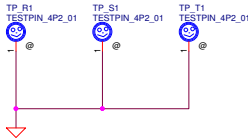
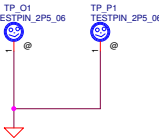
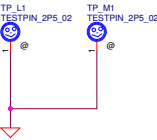
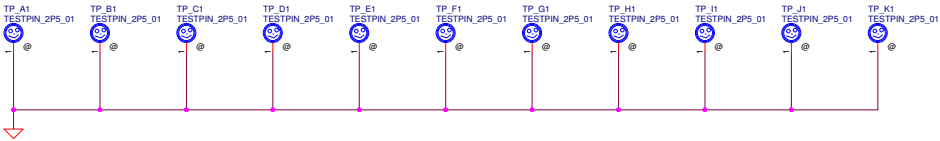
SDV EC011 DCDC



| | | | | |
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| | | | LA-E292P | |

PTH FOR SCREW HOLE

| Value | Hole Dia | Pad Dia | | QTY |
|----------------|----------|---------|--------|-----|
| | | TOP | BOTTOM | |
| TESTPIN_2P5_01 | 2.5 | 6 | 6 | 11 |
| TESTPIN_2P5_02 | 2.5 | 7.4 | 7.4 | 2 |
| TESTPIN_2P5_03 | 2.5 | Square | 0 | 1 |
| TESTPIN_2P5_06 | 2.5 | 5 | 5 | 2 |
| TESTPIN_2P8_01 | 2.8 | 0 | Square | 1 |
| TESTPIN_4P3_01 | 4.3 | 6.5 | 6.5 | 3 |
| TESTPIN_4P0_01 | 4.0 | 6.1 | 6.1 | 4 |



<https://vinafix.com>

FID
Board Area

FD1
NC, NO CONNECT TO ANY.

FD4
NC, NO CONNECT TO ANY.

FD2
NC, NO CONNECT TO ANY.

FD3
NC, NO CONNECT TO ANY.

| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|-----------------------|
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| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | Title | |
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| | | | | Document Number | 0.5 |
| | | | | Custom | LA-E292P |
| | | | | Date | Tuesday, May 03, 2016 |
| | | | | Sheet | 74 of 75 |

ZZZ
DAB001BL000
DIMM

ZZZ1
DAB001BM000
On board

U58
KBL OKKS 2.4G
CPU1@
SA00009PJ40

U153
Jacksonville WGI219V
NVPRO@
SA000095410

<https://vinafix.com>

| | | | | | |
|---|--------------------|-----------------|------------|--|----------------|
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| Issued Date | 2014/11/04 | Deciphered Date | 2016/12/31 | Title | PCB CPU PN |
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